BIO DATA

Name	: **PRITHA BANERJEE**
Permanent Position	: Assistant Professor, Department of Computer Science and Engineering, University of Calcutta, Kolkata, India
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Date of birth	: September 10, 1974.

Academic Qualifications:

1. Ph. D. in Computer Science from **Indian Statistical Institute**, Kolkata, India, February, 2011; Thesis Title: *Fast Placement and Floorplanning Methods in Modern Reconfigurable FPGAs.*

2. Master of Computer Science from Interdisciplinary School of Scientific Computing, **University of Pune**, 1998. (I^{st} Division Distinction with 75.8% marks).

3. Bachelor of Computer Science from Fergusson College, under **University of Pune**, 1996. (I^{st} Division Distinction with 76.25% marks).

4. Higher Secondary from Tamil Nadu Board of Higher Secondary Education, 1993. (with 90.0% marks)

5. Madhyamik from West Bengal Board of Secondary Education, 1991. (I^{st} division with 78.5% marks)

Awards:

- Received *Student Innovative Potential Award 2011* from Indian National Academy of Engineering (INAE) for the Ph. D Thesis titled *Fast Placement and Floorplaning Methods in Modern Reconfigurable FPGAs*
- Received National Scholarship for Madhyamik Exam (After class X), 1991

Work Experience:

(W1) Continuing working as Assistant Professor, Department of Computer Science & Engineering, University of Calcutta, Kolkata, India after completion of Post-doctoral studies.

(W2) Completed one year of Post-doctoral Studies at Graduate Institute of Electronics Engineering (GIEE), National Taiwan University, Taipei, Taiwan (taking study leave from University of Calcutta) from October 2011 to October 2012.

(W3) Joined University of Calcutta in the permanent position of an Assistant Professor, Department of Computer Science & Engineering, on December 1, 2009 and worked till October 2011

(W4) Project linked researcher in the project titled *Techniques for Robust Physical Design in Nanometer ICs* at Advanced Computing and Microelectronics Unit, Indian Statistical Institute, Kolkata, from June, 2009 to Nov, 2009.

(W5) Project linked research person (Senior Computer Engineer) in an Intel funded project *Delay Fault Modeling and Test Pattern Generation for Power Supply Noise* at Advanced Computing and Microelectronics Unit, Indian Statistical Institute, Kolkata, from April 2007 to April 2009.

(W6) Senior Research Fellow at Advanced Computing and Microelectronics Unit, Indian Statistical Institute, Kolkata from February 2004 to January 2007.

(W7) Junior Research Fellow at Advanced Computing and Microelectronics Unit, Indian Statistical Institute, Kolkata from February 2002 to January 2004.

(W8) Project linked person (Research Fellow) in an Indo-French project titled *Compilation and Optimization of Reconfigurable Co-processors* at Advanced Computing and Microelectronics Unit, Indian Statistical Institute, Kolkata, from March 2000 to January 2002.

(W9) Associate in a software consultancy firm, SNR Consulting Pvt. Ltd., Pune, India from July 1998 to February 2000.

Research Experience :

- VLSI physical design algorithms
- Placement and floorplanning algorithm for Field Programmable Gate Arrays (FPGA)
- Graph theoretic applications in VLSI and FPGA domain
- Manufacturability aware physical design

Teaching Experience :

- Teaching VLSI Design, Computational Geometry, Computational Mathematics, Data Structures, Design and analysis of Algorithms at Department of Computer Science and Engineering, University of Calcutta since Jan. 2010.
- Taught Logic Design for undergraduate student (BCA) and Object oriented programming for post graduate students (M.Sc. Bioinformatics) at BIT, Mesra- Kolkata Center for one semester July-December, 2008.
- Worked as Teaching Assistant for one semester *VLSI Design and Algorithms* course for M. Tech students at Indian Statistical Institute, Kolkata.
- Conducted a full semester Laboratory course on *VLSI Design* at Department of Computer Science and Engineering, Kalyani University, Nadia, West Bengal, India, from July 2007 to December 2007.
- Delivered lectures on *FPGA Placement and Routing* in Nov. 2005 as a resource person for the UGC Refresher Course in Computer Science held at Jadavpur University, Kolkata, West Bengal, India.
- Delivered lectures on *VLSI Physical Design Algorithms* in Nov. 19-23, 2003 as a resource person for the UGC Refresher Course in Computer Science held at Department of Computer Science, Shivaji University, Kolhapur, Maharashtra, India.

International Visits / Workshops attended:

(V1) Visited Prof. Yao-Wen Chang, Graduate Institute of Electronics Engineering, National Taiwan University as Post-doc during 2011-2012 and as Co-PI of a Indo Taiwan collaborative Project during July 2014, and March 2016

(V2) Visited Prof. David Z. Pan, Dept. of Electrical and Computer Engineering, University of Texas at Austin, USA during August 2014

(V3) Visited Prof. Srinivas Katkoori, Department of Computer Science and Engineering, University of South Florida, Tampa, USA, durig August 2014

(V4) Delivered a seminar titled "Floorplanning for Partial Reconfiguration in FPGAs" at *Imperial College, London*, UK in May, 2009.

(V5) Presented the thesis poster titled "Faster Placement and Floorplanning in FPGAs" in *Intl. Conference on Design Automation and Test in Europe (DATE 2009)*, Nice, France.

(V6) Delivered a seminar titled "Accelerators for FPGA Placement" at *ITIV, University of Karlsruhe*, Germany in August, 2005.

(V7) Presented the paper titled "Fast FPGA Placement using Space-filling Curve" in *Intl. Conference on Field Programmable Logic and Applications (FPL 2005)*, Tampere, Finland.

(V8) Attended *An Asian Course on Microprocessor Laboratory on Advanced VLSI Design Techniques Using Hardware Description Language* at Manila, Philippines, from Nov. 25 to Dec. 13, 2002, organized by the *Abdus Salam International Centre for Theoretical Physics(ICTP)*, Trieste, Italy.

Past Projects:

- Co-Principal Investigator of the Indo-Taiwan collaborative research project "Lithography aware physical design for below 20 nm process technology" with Prof. Susmita Sur-Kolay, Indian Statistical Institute, Kolkata, India and Prof. Yao-Wen Chang, GIEE, National Taiwan University, Taipei, Taiwan, funded by DST, India and NSC, Taiwan for the period 2013-2016.

Other Activities:

1. Member, IEEE
2. Member, ACM

List of Publications:

Refereed Journals

(J1) **Pritha Banerjee**, Megha Sangtani and Susmita Sur-Kolay,"Floorplanning for Partially Reconfigurable FPGAs", *IEEE Trans. on Computer Aided Design of Integrated circuits and Systems*, vol. 30, no. 1, pp. 8-17, January 2011.

(J2) **Pritha Banerjee**, Debasri Saha and Susmita Sur-Kolay," Cone-based placement for Field Programmable Gate Arrays", *IET Computer and Digital Techniques*, vol. 5, issue 1, pp. 49-62, January 2011.

(J3) **Pritha Banerjee**, Susmita Sur-Kolay, Arijit Bishnu, Sandip Das, Subhas C. Nandy and Subhasis Bhattacharjee, "FPGA Placement using Space Filling Curves: Theory Meets Practice", Special issue on Configuring Algorithms, Processes and Architecture (CAPA) in *ACM Transactions on Embedded Computing System (TECS)*, vol. 9, no. 2, Article no. 12, pp. 1-23, October 2009.

(J4) **Pritha Banerjee**, Susmita Sur-Kolay and Arijit Bishnu, "Fast Unified Floorplan Topology Generation and Sizing on Heterogeneous FPGAs", *IEEE Trans. on Computer Aided Design of Integrated circuits and Systems*, vol. 28, no. 5, pp. 651-661, May 2009.

Refereed Conference Proceedings

(C1) S. Paul, **P. Banerjee** and S. Sur-Kolay, "Minimization of Flare in EUVL by Simultaneous Wire Segment Perturbation and Dummification", in *2019 IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, Miami, FL, USA, 2019, pp. 212-217.

(C2) S. Paul, **P. Banerjee** and S. Sur-Kolay, "Post-Layout Perturbation towards Stitch Friendly Layout for Multiple E-Beam Lithography", in *ICCD* 2017, pp. 411-414

(C3) S. Paul, **P. Banerjee** and S. Sur-Kolay, "Flare reduction in EUV Lithography by perturbation of wire segments,", in *2015 IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC)*, Daejeon, 2015, pp. 7-12.

(C4) S. Paul, R. Das and **P. Banerjee**, "A study on detailed placement for FPGAs,", in *International Conference on VLSI Systems, Architecture, Technology and Applications (VLSI-SATA), 2015*, Bangalore, 2015, pp. 1-6.

(C5) Aparna Das,Mousumi Ghosh,**Pritha Banerjee**, Soumya Pandit, "Power Aware Clustering and Placement for FPGAs", in *Proc. of 1st International Science and Technology Congress 2014 (IEM-CONGRESS 2014), Elsevier: Science :: Technology, ISBN: 9789351072485*, Kolkata, India, August 28-31, 2014, p-53.

(C6) Tzu-Hen-Lin, **Pritha Banerjee**, Yao-Wen Chang, "An Efficient and Effective Analytical Placer for FPGAs", in *Design Automation Conference*, Austin, TX, USA, 2-6 June, 2013.

(C7) Sagnik Mukhopadhyay,**Pritha Banerjee**, Susmita Sur-Kolay, "Balanced Bipartitioning of a Multiweighted Hypergraph for Heterogeneous FPGAs", in *Proc. of VII Southern Programmable Logic (SPL) Conference*, 13-15 April 2011, Cordoba, Argentina.

(C8) **Pritha Banerjee**, Megha Sangtani and Susmita Sur-Kolay, "Floorplanning for Partial Reconfiguration in FPGAs", in *Proc. of the* 22^{nd} *International Conference on VLSI Design*, IEEE CS Press, January 2009, New Delhi, India.

(C9) Debasri Saha, **Pritha Banerjee** and Susmita Sur Kolay, "Fast I/O Pad Placement in FPGAs", in *Progress in VLSI Design and Test*, 11^{th} VLSI Design And Test Symposium, pp. 153-161, August 2007, Kolkata, India.

(C10) **Pritha Banerjee** and Susmita Sur-Kolay, "Faster Placer for Island-style FPGAs", in *Proc. of International Conference on Computing: Theory and Applications*, IEEE CS Press, pp. 117-121, March 2007, Kolkata, India.

(C11) **Pritha Banerjee**, Susmita Sur-Kolay and Arijit Bishnu, "Floorplanning in Modern FPGAs" in *Proc. of the* 20^{th} *International Conference on VLSI Design*, IEEE CS Press, pp. 893-898, January 2007, Bangalore, India.

(C12) **Pritha Banerjee**, Subhais Bhattacharjee, Susmita Sur-Kolay, Sandip Das and Subhas C. Nandy, "Fast FPGA Placement using Space-filling Curve", in *Proc. of the* 15^{th} *International Conference on Field Programmable Logic and Applications (FPL)*, IEEE CS Press, pp. 415-420, August 2005, Tampere, Finland.

(C13) **Pritha Banerjee** and Susmita Sur Kolay, "An Accelerator for FPGA Placement", in *Progress in VLSI Design and Test*, 6^{th} VLSI Design and Test Workshops, pp. 340-347, August 2002, Bangalore, India.

Others

1. Tzu-Hen Lin, **Pritha Banerjee**, and Yao-Wen Chang, "An Efficient Analytical Placement For FPGA Designs", in Proc. of 23^{rd} VLSI Design/CAD Symposium 2012, Kenting, Taiwan.