Curriculum Vitae

- **Name:** Abhijit Mallik
- **Specialization:** Microelectronics.
- **Designation:** Professor
- **Affiliation & Contact Information:**

University of Calcutta

Department of Electronic Science

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- **Past Affiliations:**
  - **Department of Electronics & Communication Engineering, Kalyani government Engineering College,** Kalyani, India, from 1997 to 2007 (initially as Assistant Professor and re-designated as Associate Professor w.e.f. 1.1.2006).
  - **Department of Electrical Engineering, Yale University, New Haven, USA**, from 1994 to 1995 as a Postdoctoral Fellow. Worked on the process development and interface characterization of jet-vapor-deposited (JVD) silicon nitride as an alternative gate insulator for ultra-large-scale-integration (ULSI) applications.
  - **Department of Electrical Engineering, Indian Institute of Technology, Bombay**, India, as a Ph.D. student. Played a key role in standardizing an nMOS process and developing a radiation-hard chip going up to 1 Mrad(Si).

- **Educational Background:**

  - **B. Sc. (Hons.) in Physics** from the University of Calcutta (Presidency College) in 1986 (session 1982-1985).

  - **M. Sc. in Electronic Science** from the University of Calcutta in 1989 (Gold Medalist for securing 1st Class 1st position) (session 1985-1987).

  - **Ph. D. in Electrical Engineering** from the Indian Institute of Technology, Bombay, in 1994.

    Ph.D. Thesis Title: Study of Reoxidized Nitrided Oxide MOS Devices for Radiation-Hard Applications.

    Ph.D. Supervisors: Late Prof. A. N. Chandorkar and Prof. J. Vasi

- **Research Interest:** CMOS Devices, FinFETs & Tunnel FET, Energy Harvesting: Triboelectric Nanogenerator (TENG), Organic- & Bio-Materials-Based Electron Devices: Memristors, RRAMs.

- **Membership of Scientific Bodies:** Senior Member: IEEE

- **Research Guidance:**

  - Postdoctoral: 02

  - Ph.D.: 15 (Completed: 11, Pursuing: 04)

- **Patent**

  A. Mallik, "Tunnel Field-Effect Transistor (TFET) with Supersteep Subthreshold Swing," US Patent No. 9748368B2 dated Aug. 29, 2017, China Patent No. CN105378929B dated 22.06.2018, PCT Application No. PCT/IB2013/056828 dated 23.08.2013.

- **Books/Book Chapters:**

  A. Book:

  1. Y. Omura, **A. Mallik,** and N. Matsuo, "MOS Devices for Low-Voltage and Low-Energy Applications" Wiley-IEEE Press, Oct. 2016.

  B. Book Chapters:

  1. Y. Omura and **A. Mallik,** "Potential of Low-Voltage Low-Energy MOS Devices in Coming Sensor Network Era," in Advances in Microelectronics: Reviews, Book Series Vol. 01, IFSA Publishing.

2. E. Datta, A. Chattopadhyay, and **A. Mallik, "**Effect of Gate Dielectric Material on the Analog Performance of a Ge-Source Tunnel FET," in The Physics of Semiconductor Devices, Proc. of IWPSD-2017, Springer Proceedings in Physics (SPPHY), volume 215, January 2019.
3. S. Tewari, A. Biswas, and **A. Mallik, "**Investigations on the Logic Circuit Behavior of Hybrid CMOSFETs Comprising InGaAs nMOS and Ge pMOS Devices with Barrier Layers" in Lecture Notes in Electrical Engineering, January 2018.

❖ List of Research Projects:

Sl. No.	Project Title	Funding Agency	Total Outlay (Rs.)	Duration/ Technical Status	Remarks
1.	Investigations of Organic Nano-Materials for Non-Volatile Memory Applications	D.S.T., Govt. of India	116.97 Lacs	3 years, completed, 2019-2022	Principal Investigator
2.	Device Design and Optimization of Complementary Tunnel FETs for Low Power Applications and Their Variability Study	SERB, D.S.T., Govt. of India	40.59 Lacs	3 years, completed, 2013-2016	Principal Investigator
3.	Study of CMOS Devices and Circuits Utilising "Beyond Silicon" Channel Materials for ULSI Applications	CSIR	9.68 Lacs	3 years, completed, 2012-2015	Co-Invesigator
4.	Study and Modeling of Tunnel Field-Effect Transistor	D.S.T., Govt. of India	33.89 Lacs	3 years, completed, 2009-2013	Principal Investigator
5.	Device Design and Modeling of Sub–45nm Schottky–Barrier MOSFETs	UGC	2.35 Lacs	3 years, completed, 2010-2013	Co-Invesigator
6.	Study and Modeling of Sub-Threshold Characteristics of Deep Sub-Micron Bulk and Thin-Film SOI CMOS Devices with and without Halo Implantation	D.S.T., Govt. of India	17.77 Lacs	3 years, completed, 2019-2022	Principal Investigator (in collaboration with Jadavpur University)
7.	Channel Engineering for Deep Sub-Micron MOSFETs	A.I.C.T.E.	8.00 Lacs	3 years, completed, 2000-2002	Principal Investigator

❖ **List of Journal Publications:**

1. S. M. Nawaz, M. Chatterjee, S. Chakrabarti, N. Sepay, and **A. Mallik**, "Realization of a highly-performing triboelectric nanogenerator utilizing molecular self-assembly," ***Nano Energy***, vol. 117, 108924, Dec. 2023. (https://doi.org/10.1016/j.nanoen.2023.108924).
2. Y. Omura and **A. Mallik,** "Theoretical model and simulations to extract chemical reaction parameters ruling resistive switching in sputter deposited silicon oxide film on Si substrate," ***Journal of Applied Physics***, vol. **134**, 065105, Aug. 2023. (https://doi.org/10.1063/5.0156183).
3. M. Saha, S. Dey, S. M. Nawaz, and **A. Mallik**, "Environment friendly resistive memory based on natural casein: Role of electrode and bio-material concentration," ***Organic Electronics***, **121**, 106869, 2023. (https://doi.org/10.1016/j.orgel.2023.106869).
4. Y. Omura and **A. Mallik,** "Simulation Study on Physical Parameters Ruling Unipolar Resistive Switching of Sputter-Deposited Silicon Oxide Film on Si Substrate," ***Solid-State Electronics***, vol. **206**, 108670, Aug. 2023. (https://doi.org/10.1016/j.sse.2023.108670).
5. N. Chakraborty, J. Ghosh, S. Goswami, A. Shaw, B. Das, **A. Mallik**, and K. K. Chattopadhyay, "Perforated Turbostratic Graphene as Active Layer in a Nonvolatile Resistive Switching Memory Device," ***ACS Applied Electronic Materials***, vol. **5**, no. 4, pp. 2131-2144, 2023. (https://doi.org/10.1021/acsaelm.3c00037).
6. S. M. Nawaz, M. Saha, N. Sepay, and **A. Mallik**, "Energy-from-waste: A triboelectric nanogenerator fabricated from waste polystyrene for energy harvesting and self-powered sensor," ***Nano Energy***, vol. 104, 107902, Dec. 2022. (https://doi.org/10.1016/j.nanoen.2022.107902).
7. P. Chakraborti, A. Biswas, and A. Mallik," High sensitivity Ge-source L-shaped tunnel BioFETs for detection of high-K biomolecules," **Microsystem Technologies**, 2022 (https://doi.org/10.1007/s00542-022-05358-w).
8. M. Sil, S. M. Nawaz, and **A. Mallik**, "On the performance of hafnium-oxide-based negative capacitance FinFETs, with and without a spacer," **Semiconductor Science and Technology, 37**, 045006 (7pp), 2022. (https://doi.org/10.1088/1361-6641/ac52b7).
9. M. Saha, S. M. Nawaz, B. K. Keshari, and **A. Mallik**, "Natural-Casein-Based Biomemristor with Pinched Current−Voltage Characteristics," **ACS Applied Bio Materials,** vol. **5**, no. 2, pp. 833–840, 2022. (https://doi.org/10.1021/acsabm.1c01188).
10. B. Das, M. Samanta, P. K. Sarkar, U. K. Gharai, **A. Mallik**, and K. K. Chattopadhyay, "Copper (II) Phthalocyanine (CuPc) Based Optoelectronic Memory Devices with Multilevel Resistive Switching for Neuromorphic Application," **Advanced Electronic Materials**, vol. **7**, issue 4, 2001079 (11pp), Apr. 2021 (**https://doi.org/10.1002/aelm.202001079**).
11. E. Datta, A. Chattopadhyay, and **A. Mallik**, "A Comparison of Analog Performance, Linearity, and Distortion Characteristics between Symmetric InGaAs and Asymmetric InGaAs/InP MOSFETs," **IEEE Trans. Electron Devices,** vol. **68**, no. 4, pp. 1570-1576, Apr. 2021.

12. M. Sil and **A. Mallik**, "On the Logic Performance of Bulk Junctionless FinFETs," **Analog Integrated Circuits and Signal Processing,** vol. **106,** pp. 467–472, Jan. 2021 (https://doi.org/10.1007/s10470-020-01782-y).

13. T. Ghosh, S. Mondal, R. Maiti, S. M. Nawaz, N. N. Ghosh, E. Dinda, A. Biswas, S. K. Maity, **A. Mallik**, and D. K. Maiti, "Complementary Amide-Based Donor-Acceptor with Unique Nano-Scale Aggregation, Fluorescence, and Bandgap Lowering Properties: a WORM Memory Device," **Nanotechnology**, vol. **32**, no. 2, p. 025208 (9pp), Jan. 2021.

14. S. M. Nawaz and **A. Mallik**, "Role of Quantum Capacitance on the Random Dopant Fluctuation Induced Threshold Voltage Variability in Junctionless InGaAs FinFETs," **Solid-State Electronics 171**, 107862, 2020.

15. E. Datta, A. Chattopadhyay, **A. Mallik**, and Y. Omura, "Temperature Dependence of Analog
    Performance, Linearity, and Harmonic Distortion for a Ge-Source Tunnel FET," **IEEE Trans. Electron Devices,** vol. **67**, no. 3, pp. 810-815, Mar. 2020.

16. E. Datta, A. Chattopadhyay, and **A. Mallik**, "Relative Study of Analog Performance, Linearity and Harmonic Distortion between Junctionless and Conventional SOI FinFETs at Elevated Temperatures," **Journal of Electronic Materials**, 1-8, 2020.

17. S. Tewari, S. De, A. Biswas, and **A. Mallik**, "Impact of Sidewall Spacer on n-InGaAs Devices and Hybrid n-InGaAs/Si CMOS Amplifiers in Deca-Nanometer Regime," **Microsystem Technologies**, vol. **26**, pp. 3077–3084, 2020 (https://doi.org/10.1007/s00542-017-3658-4).

18. M. Sil, S. Guin, S. M. Nawaz, and **A. Mallik**, "Performance of Ge p-channel junctionless FinFETs for logic applications," **Applied Physics A 125**, 782, 2019.

19. Y. Jiang, S. Sato, Y. Omura, and **A. Mallik**, "Analysis of Miller Capacitance of Si Tunnel Field-Effect Transistors and Potential for Low-Voltage/Low-Energy Applications," **International Journal of Engineering Applications,** vol. **7**, No. 3, pp. 88-96, 2019.

20. S. De, S. Tewari, S. De, A. Biswas, **A. Mallik**, "Improved digital performance of hybrid CMOS inverter with Si p-MOSFET and InGaAs n-MOSFET in the nanometer regime," **Microelectronic Engineering**, vol. **211**, pp. 18-25, 2019.

21. R. Basak, B. Maiti, and **A. Mallik**, "Effect of the Presence of Trap States in Oxides in Modeling Gate Leakage Current in Advanced MOSFET with Multi-Oxide Stack," **Superlattices and Microstructures**, vol. 129, pp. 193-201, 2019.

22. Y. Omura, Y. Mori, S. Sato, and **A. Mallik**, "Revisiting the Role of Trap-Assisted-Tunneling Process on Current-Voltage Characteristics in Tunnel Field-Effect Transistors," **Journal of Applied Physics,** vol. **123**, pp. 161549-1-161549-6, Apr. 2018 (https://doi.org/10.1063/1.5010036).

23. D. K. Maiti, S. Debnath, S. M. Nawaz, B. Dey, E. Dinda, D. Roy, S. Ray, **A. Mallik**, and S. A. Hussain, "Composition-Dependent Nanoelectronics of Amido-Phenazines: Non-Volatile RRAM and WORM Memory Devices," **Scientific Reports 7**, Article number: 13308, Oct. 2017.

24. S. De, S. Tewari, A. Biswas, and **A. Mallik**, "Impact of Channel Thickness and Spacer Length on Logic Performance of p-Ge/n-Si Hybrid CMOSFETs for ULSI Applications," **Superlattices and Microstructures**, vol. 109, pp. 316-323, Sep. 2017.

25. Y. Mori, S. Sato, Y. Omura, A. Chattopadhyay, and **A. Mallik**, "On the Definition of Threshold Voltage for Tunnel FETs," **Superlattices and Microstructures**, vol. 107, pp. 17-22, Jul. 2017.

26. S. Guin, M. Sil, and **A. Mallik**, "Comparison of Logic Performance of CMOS Circuits Implemented with Junctionless and Inversion-Mode FinFETs," **IEEE Trans. Electron Devices**, vol. 64, no. 3, pp. 953-959, Mar. 2017.

27. Y. Mori, S. Sato, Y. Omura, and **A. Mallik**, "Proposal of the Possible Method to Define the Threshold Voltage of Lateral Tunnel Field-Effect Transistors," Technology Reports of Kansai University *(Osaka, Japan*), vol. 59, pp. 75-81, Mar. 2017.

28. S. M. Nawaz and **A. Mallik**, "Effects of Device Scaling on the Performance of Junctionless FinFETs Due to Gate-Metal Work Function Variability and Random Dopant Fluctuations," **IEEE Electron Device Letters,** vol. 37, no. 8, pp. 958-961, Aug. 2016.

29. S. Tewari, A. Biswas, and **A. Mallik**, "Impact of a Spacer Layer on the Analog Performance of Asymmetric InP/InGaAs nMOSFETs," **IEEE Trans. Electron Devices,** vol. 63, no. 6, pp. 2313-2320, Jun. 2016.

30. S. M. Nawaz, S. Dutta, and **A. Mallik**, "Comparison of Gate-Metal Work Function Variability Between Ge and Si p-Channel FinFETs," **IEEE Trans. Electron Devices,** vol. 62, no. 12, pp. 3951-3956, Dec. 2015.

31. S. M. Nawaz, S. Dutta, and **A. Mallik**, "A Comparison of Random Discrete Dopant Induced Variability between Ge and Si Junctionless p-FinFETs," **Applied Physics Letters**, vol. 107, no. 3, pp. 033506-1-033506-4, Jul. 2015.

32. H. Lv, S. Sato, Y. Omura, and **A. Mallik**, "Analytically Modeling the Asymmetric Double Gate Tunnel FET," **ECS Transactions,** vol. 66, no. 5, pp. 193-200, 2015.

33. S. Sato, Y. Omura, and **A. Mallik**, "Compact Model for Nano-Wire Tunnel Field-Effect Transistor," **ECS Transactions**, vol. 66, no. 5, pp. 171-177, 2015.

34. A. Chattopadhyay, **A. Mallik**, and Y. Omura, "Device Optimization and Scaling Properties of a Gate-on-Germanium Source Tunnel Field-Effect Transistor," **Superlattices and Microstructures**, vol. 82, pp. 415-429, Jun. 2015.

35. S. Tewari, A. Biswas, and **A. Mallik**, "Performance of CMOS with Si p-MOS and Asymmetric InP/InGaAs n-MOS for Analog Circuit Applications," **IEEE Trans. Electron Devices**, vol. 62, no. 5, pp. 1655-1658, May 2015.

36. R. Basak, B. Maiti, and **A. Mallik**, "Analytical Model of Gate Leakage Current Through Bilayer Oxide Stack in Advanced MOSFET," **Superlattices and Microstructures**, vol. 80, pp. 20-31, Apr. 2015.

37. S. Tewari, A. Biswas, and **A. Mallik**, "Investigation on High Performance CMOS with p-Ge and n-InGaAs MOSFETs for Logic Applications," **IEEE Trans. Nanotechnology**, vol. 14, no. 2, pp. 275-281, Mar. 2015.

38. **A. Mallik**, A. Chattopadhyay, and Y. Omura, "Gate-on-Germanium Source Tunnel Field-Effect Transistor Enabling Sub-0.5-V Operation," **Japanese Journal of Applied Physics,**, vol. 53, no. 10, pp. 1042011-1042017, Oct. 2014.

39. S. Guin, A. Chattopadhyay, A. Karmakar, and **A. Mallik**, "Impact of a Pocket Doping on the Device Performance of a Schottky Tunneling Field-Effect Transistor," **IEEE Trans. Electron Devices**, vol. 61, no. 7, pp. 2515-2522, Jul. 2014.

40. S. M. Nawaz, S. Dutta, A. Chattopadhyay, and **A. Mallik**, "Comparison of Random Dopant and Gate-Metal Workfunction Variability Between Junctionless and Conventional FinFETs," **IEEE Electron Device Letters**, vol. 35, no. 6, pp. 663-665, Jun. 2014.

41. S. Tewari, P. K. Saha, A. Biswas, and **A. Mallik**, "Effects of Barrier Layer of Nanoscale InGaAs-Channel MOSFETs on Analog Circuit Performance," *An International Journal of Jaipur National University (INROADS) (Special Issue),* vol. 3, no. 1, pp. 168-172, Jan.-Jun. 2014.

42. S. Tewari, A. Biswas, and **A. Mallik**, "High Performance Logic Gates Built with Hybrid p-Ge/ n-InGaAs CMOS Inverters at Channel Length of 45 nm," *An International Journal of Jaipur National University (INROADS) (Special Issue),* vol. 3, no. 1, pp. 357-362, Jan-June, 2014.

43. **A. Mallik**, "Tunnel FETs for Mixed-Signal System-On-Chip Applications," **ECS Transactions**, vol. 53, issue 5, pp. 93-104, May 2013.

44. S. Tewari, A. Biswas, and **A. Mallik**, "Impact of Different Barrier Layers and In-Content of the Channel on the Analog Performance of InGaAs MOSFETs," **IEEE Trans. Electron Devices**, vol. 60, no. 5, pp. 1584-1589, May 2013.

45. **A. Mallik**, A. Chattopadhyay, S. Guin, and A. Karmakar, "Impact of a Spacer-Drain Overlap on the Characteristics of a Silicon Tunnel Field-Effect Transistor Based on Vertical Tunneling," **IEEE Trans. Electron Devices**, vol. 60, no. 3, pp. 935-943, Mar. 2013.

46. S. Tewari, A. Biswas, and **A. Mallik**, "Effects of a Barrier Layer in InGaAs Channel MOSFETs for Analog/Mixed Signal System-on-Chip Applications," **International Journal of Electrical and Electronics Engineering**, vol. 2, pp. 41-44, 2013.

47. **A. Mallik** and A. Chattopadhyay, "Observation of Current Enhancement Due to Drain-Induced Drain Tunneling in Tunnel Field-Effect Transistors," **Japanese Journal of Applied Physics**, vol. 51, no. 8, pp. 0843011-0843014, Aug. 2012.

48. **A. Mallik** and A. Chattopadhyay, "Tunnel Field-Effect Transistors for Analog/Mixed-Signal System-on-Chip Applications," **IEEE Trans. Electron Devices**, vol. 59, no. 4, pp. 888-894, Apr. 2012.

49. S. Tewari, A. Biswas, and **A. Mallik**, "Study of InGaAs Channel MOSFETs for Analog/Mixed-Signal System-on-Chip Applications," **IEEE Electron Device Letters**, vol. 33, no. 3, pp. 372-374, Mar. 2012.

50. **A. Mallik** and A. Chattopadhyay, "The Impact of Fringing Field on the Device Performance of a P-Channel Tunnel Field-Effect Transistor with a High-κ Gate Dielectric," **IEEE Trans. Electron Devices**, vol. 59, no. 2, pp. 277-282, Feb. 2012.

51. **A. Mallik** and A. Chattopadhyay, "Drain-Dependence of Tunnel Field-Effect Transistor Characteristics: The Role of the Channel," **IEEE Trans. Electron Devices**, vol. 58, no. 12, pp. 4250-4257, Dec. 2011.

52. S. Chakraborty, **A. Mallik,** and C. K. Sarkar, "Subthreshold Performance of Pocket-Implanted Silicon-On-Insulator CMOS Devices and Circuits for Ultra-Low-Power Analogue/Mixed-Signal Applications," **IET Circuits Devices and Systems**, vol. 5, no. 4, pp. 343–350, July 2011.

53. A. Chattopadhyay and **A. Mallik,** "Impact of a Spacer Dielectric and a Gate Overlap/Underlap on the Device Performance of a Tunnel Field-Effect Transistor," **IEEE Trans. Electron Devices**, vol. 58, no. 3, pp. 677-683, Mar. 2011.

54. P. Sarkar, **A. Mallik,** and C. K. Sarkar, "Study on the Performance of Sub 100nm LACLATI MOSFETs for Digital Applications," **Microelectronics Reliability**, vol. 49, no. 4, pp. 392-396, Apr. 2009.

55. P. Sarkar, **A. Mallik,** and C. K. Sarkar, "Single Halo SDODEL n- MOSFET: An Alternative Low Cost Pseudo-SOI with Better Analog Performance," **Semiconductor Science and Technology**, vol. 24, no.3, 035001 (6pp), Mar. 2009.

56. S. Chakraborty, **A. Mallik,** and C. K. Sarkar, "Subthreshold Performance of Dual Material Gate CMOS Devices and Circuits for Ultralow Power Analog/Mixed-Signal Applications," **IEEE Trans. Electron Devices**, vol. 55, no. 3, pp. 827-832, Mar 2008.

57. S. Baishya, **A. Mallik,** and C. K. Sarkar, "A Threshold Voltage Model for Short-Channel MOSFETs Taking into Account the Varying Depth of Channel Depletion Layers Around the Source and Drain," **Microelectronics Reliability**, vol. 48, no. 1, pp. 17-22, Jan. 2008.

58. S. Baishya, **A. Mallik,** and C. K. Sarkar, "A Pseudo Two-Dimensional Subthreshold Surface Potential Model for Dual-Material Gate MOSFETs," **IEEE Trans. Electron Devices**, vol. 54, no. 9, pp. 2520-2525, Sep. 2007.

59. S. Baishya, **A. Mallik,** and C. K. Sarkar, "A Surface Potential Based Subthreshold Drain Current Model for Short-Channel MOS Transistors," **Semiconductor Science and Technology**, vol. 22, no.9, pp. 1066-1069, Sep. 2007.

60. P. Sarkar, **A. Mallik,** and C. K. Sarkar, "Performance Comparison of Channel Engineered Deep Sub-Micrometer Pseudo SOI n-MOSFETs," **Microelectronics Reliability**, vol. 47, no. 6, pp. 953-958, Jun. 2007.

61. S. Baishya, **A. Mallik,** and C. K. Sarkar, "Subthreshold Surface Potential and Drain Current Models for Short-Channel Pocket-Implanted MOSFETs," **Microelectronic Engineering**, vol. 84, no. 4, pp. 653-662, Apr. 2007.

62. S. Chakraborty, **A. Mallik,** C. K. Sarkar, and V. R. Rao, "Impact of Halo Doping on the Subthreshold Performance of Deep-Submicrometer CMOS Devices and Circuits for Ultralow Power Analog/Mixed-Signal Applications," **IEEE Trans. Electron Devices**, vol. 54, no. 2, pp. 241-248, Feb. 2007.

63. S. Baishya, S. Chakraborty, **A. Mallik,** and C. K. Sarkar, "A Subthreshold Surface Potential and Drain Current Model for Lateral Asymmetric Channel (LAC) MOSFET," **IETE Journal of Research (Special issue on Nanoelectronic Devices and Technology),** vol. 52, no. 5, pp. 379-390, Sep.-Oct. 2006.

64. S. Baishya, **A. Mallik,** and C. K. Sarkar, "A Subthreshold Surface Potential Model for Short Channel MOSFET Taking into Account the Varying Depth of Channel Depletion Layer Due to Source and Drain Junctions," **IEEE Trans. Electron Devices**, vol. 53, no. 3, pp. 507-514, Mar. 2006.

65. **A. Mallik,** X. W. Wang, T. P. Ma, G. J. Cui, T. Tamagawa, B. L. Halpern, and J. J. Schmitt, "Interface Traps in Jet-Vapor-Deposited Silicon Nitride-Silicon Capacitors," **Journal of Applied Physics,**, vol. 79, no. 11, pp. 8507-8511, Jun. 1996.

66. **A. Mallik,** A. N. Chandorkar, and J. Vasi, "Capture Cross-Section of Hole Traps in Reoxidized Nitrided Oxide Measured by Irradiation," **Solid-State Electronics**, vol. 38, no. 10, pp. 1851-1853, Oct. 1995.

67. **A. Mallik,** J. Vasi, and A. N. Chandorkar, "Electron Trapping During Irradiation in Reoxidized Nitrided Oxide," **IEEE Trans. Nuclear Science**, vol. 40, no. 6, pp. 1380-1387, Dec. 1993.

68. **A. Mallik**, J. Vasi, and A. N. Chandorkar, "A Study of Radiation Effects on Reoxidized Nitrided Oxide MOSFETs, Including Effects on Mobility," **Solid-State Electronics**, vol. 36, no. 9, pp. 1359-1361, Sep. 1993.

69. **A. Mallik,** J. Vasi, and A. N. Chandorkar, "The Nature of the Hole Traps in Reoxidized Nitrided Oxide Gate Dielectrics," **Journal of Applied Physics,**, vol. 74, no. 4, pp. 2665-2668, Aug. 1993.

70. A. Phanse, D. Sharma, **A. Mallik,** and J. Vasi, "Carrier Mobility Degradation in Metal-Oxide-semiconductor Field-Effect Transistors Due to Oxide Charge," **Journal of Applied Physics**, vol. 74, no. 1, pp. 757-759, Jul. 1993.

❖ List of Invited Talk/Lectures

- National Conference on Recent Developments in Nanoscience & Nanotechnology (NCRDNN 2019)" Jan. 29-31, 2019.

- 3rd international conference "2019 Devices for Integrated Circuit (DevIC)", Kalyani Government Engineering College, March 23-24, 2019
- IEEE IMFEDK, Kyoto, Japan, Jun. 2018.
- UGC-HRDC Special Winter School, C.U., Mar. 2018.
- UGC-HRDC Winter School, C.U., Feb. 2017.
- STTP course on "Emerging devices and VLSI physical design" National Institute of Technology, Silchar, Oct. 2016.
- Workshop on "Nano-materials and Devices for Biomedical Applications," CRNN, Calcutta University, Oct. 2016.
- Faculty Development Program on "Modern Trends in Communication & Circuit Design, 2016 (MTCCD, 2KH)," Narula Institute of Technology, Kolkata, October, 2016.
- Refresher course on "Nanodevices and Low-Power VLSI Design", Jadavpur University, December 2013.
- Kansai University, Osaka, Japan, June 2013.
- 223rd ECS Meeting, Toronto, Canada, May 2013.
- UGC summer school, Department of Radio Physics and Electronics, University of Calcutta, May 2012.
- Visvesvaraya National Institute of Technology, Nagpur, September 2010.
- MHRD/AICTE sponsored summer school on "Nanotechnology for Electronic and Photonic Applications" at the Kolkata Campus of IIT-Kharagpur, July, 2009.
- UGC summer school on "NanoDev-09" Department of Radio Physics and Electronics, University of Calcutta, June, 2009.
- MHRD/AICTE summer school on "Nanoelectronics: Science, Nanotechnology, Engineering & Applications" at the Kolkata Campus of IIT-Kharagpur, June, 2008.
- UGC summer school on "Semiconductor Nanoelectronics- 2008" Department of Radio Physics and Electronics, Calcutta University, June, 2008.

❖ **Foreign Visits:**

- Yale University, New Haven, Connecticut, USA, 1994-95 (Postdoctoral Fellow).
- Toronto, Canada, May 2013 (to deliver invited talk at the 223rd ECS meeting).
- Osaka Japan, June 2013 (to present a paper in *IEEE IMFEDK-2013* and to deliver a talk at the Kansai University).
- Kyoto, Japan, June 2018 (to deliver invited talk in *IEEE IMFEDK-2013).*