Curriculum Vitae of Prof. Abhijit Biswas

1. Academic qualification:

Ph. D. (Semiconductor Physics, Devices and Circuits), Department of Radio Physics and Electronics, University of Calcutta, **INDIA** (2005)
B. Tech. and M. Tech. in Radio Physics and Electronics, University of Calcutta, **INDIA**

2. Research Interests:

Semiconductor Devices, Circuits, Optoelectronics and Photovoltaics

3. Teaching Experience: 25 years as a University Faculty Member

(i) Working as a Professor in University of Calcutta since 2012 –Till date

(ii) Worked as the Head of the Department in Radio Physics and Electronics, University of Calcutta since December 2020 – December 2022.

4. Ph. D. Thesis supervised:

(i) Ms. Jayanti Paul (2022), "Ge and GeSn Channel MOSFETs and Their Performance Improvement Through BOX Engineering"
(ii)Mr. Mainak Saha, (2022), "Performance Improvement of Nitride-Based Light-Emitting Diodes"
(iii) Mr. Arnab Laha (2021), "Application-Specific Optical Systems Hosting Exceptional Singularities"
(iv) Ms. Suchismita De (2021), "Performance of Nanoscale MOSFETs Using High Mobility Semiconductors"
(v) Mr. Himanshu Karan (2020), "Studies on nitride based light-emitting diodes for solid-state lighting"
(vi) Ms. Suchismita Tewari (2017), "Study of InGaAs n-channel MOSFETs for analog/mixed signal application"
(vii) Ms. Chandrima Mondal (2016), "Studies on nanoscale Ge channel MOSFETs for analog and logic applications"
(viii) Mr. Partha Sarathi Das (2014), "Studies on high-k gate dielectrics on GaAs substrates"
(ix) Ms. Swagata Bhattacherjee (2012), "Studies of device parameters of nanoscale double gate Si & Ge MOSFETs"
(x) Mr. Pinaki Chakraborty (2010), "Modeling and characterization of non-volatile flash memory devices"

5. Sponsored Research Projects:

(i) Title: *Study of CMOS devices and circuits utilising "beyond silicon" channel materials for ULSI applications*

Principal Investigator: Prof. A. Biswas, Co-Investigator: Prof. A. Mallik
Funded by CSIR (2012-2015)

(ii) Title: *Studies on Nitride-based Light-emitting Diodes for Achieving Augmented Performance*
Principal Investigator: Prof. A. Biswas
Funded by SERB (2013-2017)

(iii) Title: *Special Manpower Development Program (SMDP) C2SD for 5 years with effect from 2015.*
Chief Investigator: Dr. S. Pandit, Co-Investigator: Prof. A. Biswas
Funded by MeitY

(iv) Title: Investigations on high mobility III-V, Ge and GeSn nano CMOS devices including radiation effects for analog/RF and logic applications
Funded by SERB (2018-2021)

6. Fellowships/Awards/Recognition/Honors:

(i). Recipient of University Grants Commission (UGC) Research Award (2012-2014)
(ii). Fellow in Institute of Engineers (FIE)
(iii). Life Member, Indian Physical Society
(iv). Life Member, The Institution of Electronics and Telecommunication Engineers (IETE), India
(v). Life Member, Forum of Scientists, Engineers & Technologists (FOSET), Kolkata
(vi). Member, IEEE Electron Device Society and Photonic Society
(vii). Post Doctoral Research Work at Interuniversity Microelectronic Center (IMEC), Belgium (2007).
(viii) Received "**Best Citizen of India Gold Medal Award**" in August 2019 from Global Economic Progress & Research Association.

7. Worked as <u>Reviewer</u> in the following Journals:

International:
(a) IEEE Electron. Device Lett.
(b) IEEE Trans. Electron Devices
(c) IEEE Journal of Quantum Electronics
(d) IEEE Trans. Nanotechnology
(e) Superlattices and Microstructures
(f) Optics & Laser Technology
(g) Microelectronics Reliability (Elsevier)
(h) Materials Science in Semiconductor Processing (Elsevier)
(i) Microsystem Technologies (Springer)
(j) IET Circuits, Devices and Systems
(k) Journal of Optical Communications
(i) Semiconductor Science and Technology

National:
(a) IETE Journal of Research
(b) Defense Science Journal

8. Working as a **Guest Editor** for the Journal ***Microsystem Technologies (Springer)*** in connection with the International Conference Micro-2018.

9. Working as a **Guest Editor** jointly with Dr. Prabir Saha for the Journal ***Microsystem Technologies (Springer)*** in connection with the International Conference Micro-2017.

10. Working as a **Guest Editor** jointly with Prof. J. K. Mondal for the Journal ***Microsystem Technologies (Springer)*** in connection with the International Conference Micro-2016.

11. My name was included in the **Golden List of Reviewers** of the ***IEEE Trans. Electron Devices*** for the following calendar year: **2014** (Ref.: Vol.**61**, No. 12, p. 3922, Dec. 2014)

12. **Worked as Ph.D. Thesis Examiner:** Jadavpur University, Visva-Bharati University, Indian Institute of Technology-BHU, NIT Rourkela, BIT Mesra and NIT Silchar.

13. Working as an **External Member** of the **Ph. D. committee** in the Department of Instrumentation and Electronics, Jadavpur University.

14. Working as a **Member of the Ph. D. committee** in the Department of Radio Physics and Electronics, University of Calcutta.

15. Conference/Workshop/Course Organized

(i) Worked as a General Chair in the 6th International Conference on Microelectronics, Circuits and Systems during July 25-26, 2020, Kolkata.

(ii) Worked as a General Chair in the 6th International Conference on Microelectronics, Circuits and Systems during July 6-7, 2019, Kolkata.

(iii) Worked as a General Chair in the 5th International Conference on Microelectronics, Circuits and Systems during May 19-20, 2018, Bhubaneswar, Odisha.

(iv) Worked as a General Chair in the 4th International Conference on Microelectronics, Circuits and Systems during June 3-4, 2017, Darjeeling, West Bengal.

(v) Worked as a Program Chair in the 3rd International Conference on Microelectronics, Circuits and Systems during July 9-10, 2016, Kolkata.

(vi) Worked as a Course Co-ordinator for the Ph. D. course work in the Department of Radio Physics and Electronics, University during June 16-30, 2016.

(vii) Worked as a Member in the 6th International Conference on Computers and Devices for Communication (*CODEC*-15), December 16-18, 2015.

(viii) Worked as a course co-ordinator for the Summer School on "Frontiers of Nano Materials, Structures and Devices (NanoMASTD), 2012" during June 20-July 10, 2012.

(ix) Worked as an associate course co-ordinator Techniques for Design, Fabrication and Computation of Integrated Circuits (TECHNOMICS-12) during May 23-June 13, 2012.

(x) Worked as a course co-ordinator for the summer school on Physics and Simulation Techniques for Nanoscale Electronic Devices NanoDev-2009 held during June 1-19, 2009.

16. Invited Talks/ Plenary Talks:

(i) Keynote Talk, *IEEE Silchar Subsection Conference (SILCON), 2022*, NIT Silchar, Assam during November 4-6, 2022.

(ii) Invited Talk, International Conference on Microelectronics, Computing & Communication Systems (MCCS) at Ranchi during November 9-10, 2019.

(iii) Invited Talk, 5th International Conference on Microelectronics, Circuits and Systems, Bhubaneswar, Odisha during May 19-20, 2018.

(iv) Invited Talk, AICTE Sponsored Short Term Training Course at IIT-BHU, Baranasi, July 17-22, 2017

(v) Invited Talk, 4th International Conference on Microelectronics, Circuits and Systems, Darjeeling during June 3-4, 2017.

(vi) Invited Talk, 5-Day tutorial cum Workshop on Nano-materials and Devices for Biomedical Applications, CRNN, Salt Lake, Kolkata, October 24-28, 2016.

(vii) Invited Talk, 3rd International Conference on Microelectronics, Circuits and Systems, Kolkata during July 9-10, 2016.

(viii) Plenary Talk, International Conference on Recent Trends in Engineering and Material Sciences (ICEMS-2016) at Jaipur National University, Jaipur, Rajathan during March 17-19, 2016.

(ix) Invited Talk, Organized by UGC-NRCPS at Tripura University, March 28, 2016.

(x) Invited Talk, International Conference on Microelectronics, Computing & Communication Systems (MCCS) at Ranchi during November 14-15, 2015.

(xi) Invited Talk, Emerging Technology Trends in Electronics, Communication and Networking (ET2ECN), SVNIT, Surat, December 26-27, 2014.

(xii) Invited Talk, Summer school on "Frontiers of Nano Materials, Structures and Devices (NanoMASTD), 2012" organized by UGC-NRCPS during June 20-July 10, 2012.

(xiii) Invited Talk, Summer School on "Techniques for Design, Fabrication and Computation of Integrated Circuits (TECHNOMICS-12)." organized by UGC-NRCPS during May 23-June 13, 2012.

(xiv) Invited Talk, Outreach program at Tezpur University organized by UGC-NRCPS during January 23-26, 2012.

(xv) Invited Talk, Outreach program at Mizoram University organized by UGC-NRCPS held during March 23-26, 2011.

(xvi) Invited Talk, Summer school on Photonics – Systems, Modeling Approach & Research Trends PhotoSMART-2010 organized by UGC-NRCPS held during June 1-18, 2010.

(xvii) Invited Talk, Summer school on Physics and Simulation Techniques for Nanoscale Electronic Devices NanoDev-2009 organized by UGC-NRCPS held during June 1-19, 2009.

(xviii) Invited Talk, Summer school Physics of Semiconductor Nanosbtructures SemiNano-2008 organized by UGC-NRCPS held during June 2-20, 2008.

17. List of Publications (Citations: 797; h-index: 16, i10-index: 29)

A. Research Papers Published/Accepted in Science Citation Index (SCI) Journals

1. K. Banerjee and **A. Biswas**, "Enhanced analog/RF performance of hybrid charge plasma based junctionless C-FinFET amplifiers at 10 nm technology node," *Microelectronics Journal*, 2022. https:// DOI: 10.1016/j.mejo.2022.105662.

2. P. Chakraborti, **A. Biswas** and A. Mallik, "High Sensitivity Ge-source L-shaped Tunnel BioFETs for Detection of High-K Biomolecules," *Microsystem Technologies*, 2022.

3. A. Roy, S. Dey, A. Laha, **A. Biswas** and S. N. Ghosh, "Exceptional Point induced asymmetric mode conversion in a dual-core optical fiber segment," *Optics Letts*, Vol. 47, pp. 2546-2549, 2022

4. D. Roy, D. P. Samajdar and **A. Biswas**, "Design of hybrid solar cell with GaAs1−xBix (x = 0.01) nanowire core and conformally coated P3HT/ITO shell," *Solar Energy*, Vol. 238, pp.1-8, 2022. https://doi.org/10.1016/j.solener.2022.04.019

5. H. Karan and **A. Biswas**, "Improving performance of light-emitting diodes using InGaN/GaN MQWs with varying trapezoidal bottom well width", *Optik*, Vol. 247, p. 167888, 2021.

6. D. Roy, D. P. Samajdar and **A. Biswas**, "Photovoltaic Performance Improvement of $GaAs_{1-x}Bi_x$Nanowire Solar Cells in Terms of Light Trapping Capability and Efficiency," *Solar Energy*, Vol. 221, pp. 468-475, 2021.

7. D. Roy and **A. Biswas**, "Design and Analysis of Ultra-Thin Dielectric Film Embedded Nanoscale Double-Gate MOSFETs for Boosting Logic Performance," *AEUE - International Journal of Electronics and Communications,* Vol. 131, pp. 153614, 2021.

8. S. Ghosh, S. Tewari, **A. Biswas**, and A. Chakrabarti, "High performance pH sensors using ion sensitive InGaAs-channel MOSFETs at sub-100 nm technology node," *J. of Electronic Materials,* Vol.50, pp.1292-1300, 2021.

9. K. Banerjee and **A. Biswas**, "Improved Digital Performance of Charge Plasma Based Junctionless C-FinFETs at 10 nm Technology Node and Beyond," *AEUE - International Journal of Electronics and Communications,* Vol. 124, pp. 153350*,* Sept. 2020.

10. P. Nath, **A. Biswas** and V. Nath, "Performance optimization of solar cells using non-polar, semi-polar and polar InGaN/GaN multiple quantum wells alongside AlGaN blocking layers," *Microsystem Technologies*, Vol. 27, pp. 301–306, 2021.

11. A. Laha, S. Dey, D. Beniwal, **A. Biswas** and S. N. Ghosh, "Third-order exceptional point and successive switching among three states in an optical microcavity," *Physical Review A,* Vol. 101(6), p-063829, 2020.

12. A. Laha, S. Dey, H. K. Gandhi, **A. Biswas** and S. N. Ghosh, "Exceptional Point and Toward Mode Selective Optical Isolation," *ACS Photonics,* Vol. 7, No. 4, pp. 967-974, 2020.

13. J. Paul, C. Mondal and **A Biswas**, "Suppression of buried oxide induced variability on digital performance of GeOI pMOSFETs using substrate bias scheme," *Microsystem Technologies*, 26, pp.1605–1611, 2020.

14. S. Bhattacherjee and **A. Biswas**, "Investigation on noise performance of $InAs_xSb_{1-x}$ MOSFETs with compositional variations," Microsystem Technologies, 26, pp.1133–1140, 2020.

15. S. Dasgupta, C. Mondal and **A Biswas**, "Effects of temperature and channel thickness on digital and analog performance of InAs quantum well nMOSFETs," Microsystem Technologies, 26, pp.1265–1271, 2020.

16. S. De, S. Tewari, and **A. Biswas**, "Negative bias temperature instability (NBTI) effects on p-Si/n-InGaAs hybrid CMOSFETs for digital applications," *Microsystem Technologies*, Vol. 26, pp.1173–1178, 2020.

17. S. Dasgupta, C. Mondal and **A Biswas**, "Role of grooving angle of 14-nm-InAs channel quantum well MOSFETs for improvement of analog/RF and linearity performance," *IET Circuits, Devices and Systems,* Vol. 13, pp. 1292 – 1298, 2019.

18. S. De, S. Tewari, **A. Biswas** and A. Mallik, "Improved digital performance of hybrid CMOS inverter with Si p-MOSFET and InGaAs n-MOSFET in the nanometer regime," *Microelectronic Engineering,* Vol. 211, pp. 18-25, 2019.

19. D. Roy and **A. Biswas,** "Effects of asymmetric underlap spacers on nanoscale JLTs and design of optimized CMOS amplifiers," *IET Circuits, Devices and Systems,* Vol. 13, pp. 510 – 518, 2019.

20. J. Paul, C. Mondal and **A Biswas**, "Subthreshold modeling of nanoscale germanium-tin (GeSn)-on-insulator MOSFETs including quantum effects," *Materials Science in Semiconductor Processing,* Vol. 94, pp. 128-135, 2019.

21. A. Laha, **A. Biswas** and S. N. Ghosh, "Minimally asymmetric state conversion around exceptional singularities in a specialty optical microcavity," *J. of Optics*, Vol. 21, 025201, 2019.

22. H. Karan, M. Saha, **A. Biswas** and D. Biswas, "Analysis of luminescence spectra of rectangular and trapezoidal InGaN/GaN multiple quantum wells under varying bias conditions," *Optical Materials*, Vol. 86, pp. 247-255, 2018.

23. N. Mondal, S. Tewari and **A. Biswas,** "Enhancement of pH-sensitivity using $In_{0.53}Ga_{0.47}As$ channel ion-sensitive-field-effect-transistors," *Microsystem Technologies*, 2018.

24. A. Laha, **A. Biswas** and S. N. Ghosh, "Non-adiabatic Modal Dynamics around Exceptional Points in an All-Lossy Dual-Mode Optical Waveguide: Towards Chirality Driven Asymmetric Mode-Conversion," *Physical Review Applied*, 2018.

25. S. Bhattacherjee and **A. Biswas**, "Effects of sidewall spacer layers on thermal and low frequency noise performance of SOI UTB MOSFETs," *Microsystem Technologies*, 2018. DOI:10.1007/s00542-018-4141-6

26. M. Saha and **A. Biswas**, "High Performance GaN/InGaN Multiple Quantum Well LEDs through Electron Blocking Layer Engineering," *Microsystem Technologies*, 2018. DOI:10.1007/s00542-018-4091-z

27. J. Paul, C. Mondal and **A Biswas**, "Enhancing digital performance of nanoscale GeOI MOSFETs through optimization of buried oxide properties and channel thickness," *Microsystem Technologies*, 2018. DOI: 10.1007/s00542-018-4113-x

28. J. Paul, C. Mondal and **A Biswas**, "Studies of buried oxide properties on nanoscale GeOI pMOSFETs for design of a high performance common source amplifier," *Materials Science in Semiconductor Processing,* Vol. 80, pp. 85-92, 2018.

29. M. Saha, **A. Biswas** and H. Karan, "Monolithic high performance InGaN/GaN white LEDs with a tunnel junction cascaded yellow and blue light-emitting structures," *Optical Materials*, Vol. 77, pp. 104-110, 2018.

30. D. Roy and **A. Biswas,** "Analytical model of nanoscale junctionless transistors towards controlling of short channel effects through source/drain underlap and channel thickness engineering," *Superlattices and Microstructures,* Vol.113, pp. 71-81, 2018.

31. S. Bhattacherjee, **A. Biswas** and S. N. Ghosh, "Less-dispersive specialty optical fiber with an enhanced operational bandgap for applications in the mid infrared region," *J. Opt. Soc. Am. B,* Vol. 35, pp. 73-80, 2018.

32. S. Tewari, S. De, **A. Biswas** and A. Mallik, "Impact of sidewall spacer on n-InGaAs devices and hybrid InGaAs/Si CMOS amplifiers in deca-nanometer regime," *Microsystem Technologies*, 2017.

33. K. Banerjee, S.Tewari, and **A. Biswas**, "Impact of aspect ratio of nanoscale hybrid p-Ge/n-Si complementary FinFETs on the logic performance," *Microsystem Technologies*, 2017.

34. A. Roy, **A. Biswas**, R. K. Varshney and S. N. Ghosh, "Highly sensitive refractive index sensor based on degeneracy in specialty optical fibers: a new approach," *Microsystem Technologies*, 2017. https://doi.org/10.1007/s00542-017-3622-3

35. H. Karan, M. Saha and **A. Biswas**, "Step multiple quantum well enabled performance enhancement in InGaN/GaN based light-emitting diodes," *Microsystem Technologies*, 2017. DOI: 10.1007/s00542-017-3567-6

36. D. Roy and **A. Biswas,** "Asymmetric underlap spacer layer enabled nanoscale double gate MOSFETs for design of ultra-wideband cascode amplifiers," *Superlattices and Microstructures,* Vol. 110, pp. 114-125, 2017.

37. P. Biswas, B. Pal, **A. Biswas** and S. N. Ghosh, "Towards self-similar propagation of optical pulses in a dispersion tailored, nonlinear and segmented Bragg fiber at 2.8 μm," *IEEE Photonics Journal*, Vol. 9, No. 4, 7104412-1-13, 2017.

38. A. Laha, **A. Biswas** and S. N. Ghosh, "Next nearest neighbor resonance coupling and exceptional singularities in degenerate optical microcavities," *Journal of the Optical Society of America B*, vol. 34, No.10, pp. 2050-2058, August 2017.

39. H. Karan, **A. Biswas** and M. Saha, "Improved performance of InGaN/GaN MQW LEDs with trapezoidal wells and gradually thinned barrier layers towards anode," *Optics Communications*, Vol. 400, pp. 89-95, 2017.

40. S. De, S. Tewari, **A. Biswas** and A. Mallik, "Impact of channel thickness and spacer length on logic performance of p-Ge/n-Si hybrid CMOSFETs for ULSI applications," *Superlattices and Microstructures,* Vol. 109, pp. 316-323, September 2017.

41. S. Bhattacherjee and **A. Biswas**, "Development of noise model for InAsSb MOSFETs and their application in low noise amplifiers," *Microsystem Technologies,* 2017. https://doi.org/10.1007/s00542-017-3466-x

42. C. Mondal and **A Biswas**, "Performance analysis of nanoscale GeSn MOSFETs for mixed-mode circuit applications," *Materials Science in Semiconductor Processing,* Vol. 66, pp. 109-116, 2017.

43. D. Roy and **A. Biswas,** "Sidewall spacer layer engineering for improvement of analog/RF performance of nanoscale double-gate junctionless transistors," *Microsystem Technologies*, Vol. 23, pp. 2847–2857, 2017.

44. P. S. Das and **A. Biswas,** "Effect of Ge interface control layer on the interfacial and electrical properties of $TaYO_x$ thin films on GaAs substrates," *Microsystem Technologies*, Vol. 23, pp. 2055-2063, 2017.

45. D. Roy and **A. Biswas**, "Performance optimization of nanoscale junctionless transistors through varying device design parameters for ultra-low power logic applications," *Superlattices and Microstructures*, Vol. 97, pp. 140-154, 2016.

46. P. Biswas, P. Adhikary, **A. Biswas** and S. N. Ghosh, "Formation and stability analysis of parabolic pulses through specialty microstructured optical fibers at 2.1 μm," *Optics Communications*, Vol. 377, pp. 120-127, 2016.

47. S. Tewari, **A. Biswas** and A. Mallik, "Impact of a Spacer Layer on the Analog Performance of Asymmetric InP/InGaAs n-MOSFETs," *IEEE Trans. Electron Devices,* Vol. 63, no. 6, pp. 2313 – 2320, 2016**.**

48. S. Bera, C. Mondal and **A. Biswas**, "Development of a Methodology for the Extraction of BSIM3v3.2.2 Parameters of Ge-Channel MOSFETs and Estimation of Analog Circuit Performance," *Microsystem Technologies*, Vol. 23, Issue 9, pp. 4123-4131, 2016.

49. S. Tewari, **A. Biswas** and A. Mallik, "Performance of CMOS with Si p-MOS and asymmetric InP/InGaAs n-MOS for analog circuit applications," *IEEE Trans. Electron Devices, Vol. 62, no. 5,* pp. 1655-1658*,* 2015**.**

50. S. Tewari, **A. Biswas** and A. Mallik, "Investigation on high performance CMOS with p-Ge and n-InGaAs MOSFETs for logic applications*," IEEE Trans. on Nanotechnology***,** Vol. 14, pp. 274-281, 2015.

51. P. S. Das and **A. Biswas,** Interface properties, physical and electrical characterization of sputtered TaAlOx on silicon-passivated n-GaAs substrates," *Appl. Phys. A***,** DOI 10.1007/s00339-014-8845-x, 2015.

52. C. Mondal and **A. Biswas**, "Binary Alloy Enabled Gate Work Function Engineering of Nanoscale UTB-GeOI MOSFETs for Mixed-Signal System-on-Chip Applications," *Superlattices and Microstructures,* Vol. 75, pp. 118–126, 2014.

53. **A. Biswas** and S. Bhattacherjee, "Temperature dependent model for threshold voltage and subthreshold slope of strained-Si channel MOSFETs with a polysilicon gate," *Microelectronics Reliability,* Vol. 54, pp. 1527-1533, 2014.

54. C. Mondal and **A. Biswas**, "2-D compact model for drain current of fully depleted nanoscale GeOI MOSFETs for improved analog circuit design," *IEEE Trans. Electron Devices*, Vol. 60, No. 8, pp. 2525-2531, 2013.

55. C. Mondal and **A. Biswas**, "Performance analysis of nanoscale germanium on insulator MOSFETs for mixed-signal system-on-chip applications," *Superlattices and Microstructures,* Vol. 63, pp. 277-288, 2013.

56. S. Tewari, **A. Biswas** and A. Mallik, "Impact of different barrier layers and indium content of the channel on the analog performance of InGaAs MOSFETs," *IEEE Trans. Electron Devices*, Vol. 60 , No. 5, pp. 1584-1589, May, 2013.

57. **A. Biswas** and S. Bhattacherjee, "Accurate modeling of the influence of back gate bias and interface roughness on the threshold voltage of nanoscale DG MOSFETs," *Microelectronics Reliability*, Vol. 53, Issue 3, pp. 363-370, 2013.

58. D. P. Bhattacharya, S. Midday, S. Nag and **A. Biswas**, "Lattice controlled transport in quantum wires at low temperatures," Physica E: Low-dimensional Systems and Nanostructures, Vol. 47, pp. 264–269, January 2013.

59. C. Mondal and **A. Biswas**, "Studies on halo implants in controlling short-channel effects of nanoscale Ge channel pMOSFETs," *IEEE Trans. Electron Devices*, Vol. 59, No. 9, pp 2338-2344, 2012.

60. S. Tewari, **A. Biswas** and A. Mallik, "Study of InGaAs-channel MOSFETs for analog/mixed-signal system-on-chip applications," *IEEE Electron Device Lett*., Vol.33 , No.3, pp. 372-374, March, 2012.

61. S. Kabi, **A. Biswas**, D. Biswas and S. K. Biswas, "Investigations on optical transitions in InAs/InP quantum dash structures," *Applied Nanoscience,* Vol. 2, Issue 3*,* pp. 371-375, 2012.

62. P.S. Das **and A. Biswas, "**Investigations on electrical characteristics and reliability properties of MOS capacitors using $HfAlO_x$ on n-GaAs substrates," *Microelectronics Reliability*, Vol. 52, pp. 112-117, 2012.

63. P.S. Das **and A. Biswas, "**Investigation of charge trapping and breakdown characteristics of sputtered-Y_2O_3 on n-GaAs substrates," *Thin Solid Films*, Vol. 520, pp. 47-52, 2011.

64. S. Bhattacherjee and **A. Biswas,** "Performance analysis of long Ge channel double gate (DG) p MOSFETs with high-k gate dielectrics based on carrier concentration formulation," *Microelectronics Reliability*, Vol. 51, pp. 1105-1112, 2011.

65. P.S. Das **and A. Biswas, "**Influence of post deposition annealing on Y_2O_3-gated GaAs MOS capacitors and their reliability issues," *Microelectronic Engineering*, Vol. 88, pp. 282-286, 2011.

66. P.S. Das **and A. Biswas, "**Charge trapping and reliability characteristics of ultra-thin $HfYO_x$ films on n-GaAs substrates," *Microelectronics Reliability*, Vol. 50 , pp. 1924-1930, 2010.

67. P.S. Das and **A. Biswas**, "Improved electrical and interfacial properties of RF- sputtered $HfAlO_x$ on n-GaAs with effective Si passivation," *Applied Surface Science*, Vol. 256, pp. 6618-6625, 2010.

68. P. S. Das, G. K. Dalapati, D. Z. Chi, **A. Biswas** and C. K. Maiti, "Characterization of Y_2O_3 gate dielectric on n-GaAs substrates," *Applied Surface Science*, Vol. 256*,* pp. 2245-2251, 2010.

69. P. S. Das, **A. Biswas** and C. K. Maiti, "Effects of an ultrathin Si passivation layer on the interfacial properties of RF-sputtered $HfYO_x$ on n-GaAs substrates," *Semiconductor Science and Technology (U. K),* Vol. 24, p. 085026 (6 pp.), 2009.

70. P. Chakraborty, S. S. Mahato, T. K. Maiti, M. K. Bera, C. Mahata, S. K. Samanta, **A. Biswas** and C. K. Maiti, "Performance improvement of flash memory using AIN as charge-trapping layer," *Microelectronics Engineering*, Vol. 86, pp. 299- 302, 2009.

71. S. Bhattacherjee and **A. Biswas**, "Modeling of threshold voltage and subthreshold slope of nanoscale DG MOSFETs," *Semiconductor Science and Technology (U. K),* Vol. 23, p. 015010 (8 pp.), 2008.

72. B. Mukhopadhyay, **A. Biswas,** P. K. Basu, G. Eneman, P. Verheyen, E. Simoen and C. Claeys, "Modeling of threshold voltage and subthreshold slope of strained–Si MOSFETs Including quantum effects," *Semiconductor Science and Technology (U. K),* Vol. 23, p. 095017 (8 pp.), 2008.

73. S. Bhattacherjee and **A. Biswas**, "Estimation of threshold voltage and subthreshold slope of extremely scaled DG MOSFETs," *IETECH Journal of Information Systems,* Vol. 2, no. 3, pp 127-132, 2008.

74. M. Basak, **A. Biswas** and P. K. Basu, "Performance analysis of a δ-doped AllInAs- GaInAs HEMT and design optimization of radio frequency MSM-HEMT transimpedance amplifier," *IETECH Journal of Communication Techniques*, Vol. 2, no. 2, p. 152-156, 2008.

75. **A. Biswas** and P. K. Basu, "Equivalent circuit models of quantum cascade lasers for SPICE simulation of steady state and dynamic response," *Journal of Optics A : Pure and Applied Optics,* Vol. 9, pp. 26-32, 2007.

76. **A. Biswas** and P. K. Basu, "Modeling of Base Transit Time in $Si/Si_{1-y-z}Ge_yC_z$ /Si HBTs and Composition Profile Design Issue for Its Minimization," *Semiconductor Science and Technology*, *U. K.,* Vol. 18, pp. 907 - 913, 2003.

77. **A. Biswas** and P. K. Basu, “An analytical approach to the modelling of intrinsic base sheet resistance in a SiGe HBT and optimal profile design considerations for its minimization,” *Semiconductor Science and Technology*, *U. K.,* Vol. 17, p.1249 –1254, 2002.

78. **A. Biswas** and P. K. Basu, “Estimated effect of germanium and carbon on the Early voltage of a $Si_{1-x-y}Ge_xC_y$ heterojunction bipolar transistor,”' *Semiconductor Science and Technology*, *U. K.,* Vol. 16, pp. 947 - 953, 2001.

79. **A. Biswas** and P. K. Basu, “Calculation of figures of merit of $Si/Si_{1-x-y}Ge_xC_y/Si$ HBTs and their optimization,” *Solid State Electronics*, *U. K.,* Vol. 45, pp. 1885 –1889, 2001.

80. **A. Biswas** and P. K. Basu, "Calculation of base transit time in Si HBTs with incorporation of C in SiGe base," *Indian Journal of Physics 75B*, Vol. 3, pp. 223-225, 2001.

B. Books/ Book Chapter Published

1. **A. Biswas**, R. S. Saxena and D. De, “Microelectronics, Circuits and Systems Select Proceedings of 7 th International Conference on Micro2020” in LNEE Springer, 2021. ISBN: 978-981-16-1569-6

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