CURRICULUM VITAE

Personal Information:

1. Name	DR. AVIK CHATTOPADHYAY
2. Father's Name	Mr. Debabrata Chattopadhyay
3. Date of Birth	15-03-1984
4. Sex	Male
5. Nationality	Indian
6. Residential Address	"Maa Siddeshwari Bhawan", 52/3 Central Road, P.O.- Shyamnagar, Dist.- 24-Pgs.(N) , PIN CODE - 743127
7. Phone No.	Mob.: 09433564748
8. Email	avikjoy@yahoo.com ; joyavik@gmail.com

Present Status :

Working as ASSISTANT PROFESSOR (since 1st March, 2016) in the Department of RADIO PHYSICS & ELECTRONICS, University of Calcutta, Kolkata, West Bengal

Educational Qualification :

Name of the Examination	Name of the Board/Council/University	Year of Passing	Class/ Division
Madhyamik (10 class)	West Bengal Board of Secondary Education	2000	1st Div.
Higher Secondary (10+2 class)	West Bengal Council of Higher Secondary Education	2002	1st Div.
B.Tech. in ECE	West Bengal University of Technology	2006	1st Class
M.Tech. in VLSI Design	Dept. of Radio Physics & Electronics, University of Calcutta	2009	1st Class 1st
Ph.D. (Tech.) *	Dept. of Radio Physics & Electronics, University of Calcutta	2013	—

*** Ph.D. degree awarded under the new UGC Guidelines, July, 2009**

Experiences:

(i) Teaching

Name of the College (University)	Department	Designation	Subjects Taught	Working Period
Adamas Institute of Technology, Barasat (West Bengal University of Technology)	Electronics and Communication Engineering **(B. Tech.)**	Lecturer (Full-time)	Basic Electronics, Solid State Devices, Instrumentation	July, 2009 to November, 2009
Birla Institute of Technology and Science, Pilani, Rajasthan (deemed to be University)	Electrical and Electronics Engineering **(B.E.)**	Assistant Professor	Electron Devices, Signals & Systems, Analog Electronics	01/08/2014 to 16/12/2015

(ii) Research

Institution	Designation	Duration
Department of Electronic Science, University of Calcutta, Kolkata	Senior Research fellow **(SRF)** in a **DST-sponsored project** on "Study and Modeling of Tunnel Field-Effect Transistor"	14/09/2009 to 24/04/2012
Department of Electronic Science, University of Calcutta, Kolkata	Senior Research fellow **(SRF)** under the Council of Scientific and Industrial Research **(CSIR)**	25/04/2012 to 31/10/2013
Department of Electronic Science, University of Calcutta, Kolkata	Research fellow **(RF)** in a **DST-sponsored project**	Dec., 2013 to Feb., 2014
Department of Electronic Science, University of Calcutta, Kolkata	DST-PURSE Research Associate **(RA)** under Department of Science and Technology (Govt. of India)	Feb., 2014 to Jul., 2014

(iii) Industrial

Name of the Company	Designation	Working Period
Cognizant Technology Solutions India Private Ltd. ,Kolkata	Programmer Analyst	October 23, 2006 to November 26, 2007

Award Received :

- First-Class First in M.Tech. (2-year VLSI Design) in 2009 from University of Calcutta (CU).
- Enjoyed **CSIR (HRDG, Govt. of India)-fellowship award** from 25/04/2012 to 31/10/2013.

Other Academic Activities :

i) Participated in the Academic Session and Hands-On Training of the 2nd International Winter School for Graduates **(IWSG 2009)**, held at **IIT-Bombay, Mumbai** during 30th Nov-5th Dec, 2009.

ii) Guided three M. Sc. final-year projects on some advanced topics of MOSFET Device, in the department of Electronic Science at Acharya Prafulla Chandra College, New Barackpore, under Barasat State University, in the academic session 2011-12 and 2013-14.

List of Publications :

(i) Journal:

1. **A. Chattopadhyay** and A. Mallik, "Impact of a Spacer Dielectric and a Gate Overlap/Underlap on the Device Performance of a Tunnel Field-Effect Transistor," ***IEEE Trans. Electron Devices,*** vol. 58, no. 3, pp. 677-683, Mar. 2011.
2. A. Mallik and **A. Chattopadhyay**, "Drain-Dependence of Tunnel Field-Effect Transistor Characteristics: The Role of the Channel," ***IEEE Trans. Electron Devices,*** vol. 58, no. 12, pp. 4250-4257, Dec. 2011.
3. A. Mallik and **A. Chattopadhyay**, "The Impact of Fringing Field on the Device Performance of a P-Channel Tunnel Field-Effect Transistor with a High-κ Gate Dielectric," ***IEEE Trans. Electron Devices,*** vol. 59, no. 2, pp. 277-282, Feb. 2012.

4. A. Mallik and **A. Chattopadhyay**, "Tunnel Field-Effect Transistors for Analog/Mixed-Signal System-on-Chip Applications", ***IEEE Trans. Electron Devices,*** vol. 59, no. 4, pp. 888-894, Aprl. 2012.

5. A. Mallik and **A. Chattopadhyay**, "Observation of Current Enhancement Due to Drain-Induced Drain Tunneling in Tunnel Field-Effect Transistors," ***Jpn. J. Appl. Phys.,*** vol. 51, no. 8, pp. 084301-1-084301-4, Aug. 2012.

6. A. Mallik, **A. Chattopadhyay,** S. Guin, and A. Karmakar, "Impact of a Spacer-Drain Overlap on the Characteristics of a Silicon Tunnel Field-Effect Transistor Based on Vertical Tunneling," ***IEEE Trans. Electron Devices,*** vol. 60, no. 3, pp. 935-943, Mar. 2013.

7. S. M. Nawaz, S. Dutta, **A. Chattopadhyay,** and A. Mallik, "Comparison of Random Dopant and Gate-Metal Workfunction Variability Between Junctionless and Conventional FinFETs," ***IEEE Electron Device Lett.***, vol. 35, no. 6, pp. 663-665, Jun. 2014.

8. S. Guin, **A. Chattopadhyay,** A. Karmakar, and A. Mallik, "Impact of a Pocket Doping on the Device Performance of a Schottky Tunneling Field-Effect Transistor," ***IEEE Trans. Electron Devices***, vol. 61, no. 7, pp. 2515 - 2522, Jul. 2014.

9. A. Mallik, **A. Chattopadhyay**, and Y. Omura, "Gate-on-germanium source tunnel field-effect transistor enabling sub-0.5-V operation," ***Jpn. J. Appl. Phys.***, vol. 53, no. 10, pp. 104201-1- 104201-7, Oct. 2014.

10. **A. Chattopadhyay**, A. Mallik, and Y. Omura, "Device optimization and scaling properties of a gate-on-germanium source tunnel field-effect transistor," ***Superlattices and Microstructures*****,** vol. 82, pp. 415-429, Mar. 2015.

11. Y. Mori , S. Sato , Y. Omura, **A. Chattopadhyay**, A. Mallik, "On the definition of threshold voltage for tunnel FETs," ***Superlattices and Microstructures*****,** vol. 107, pp. 17-27, July 2017.

(ii) <u>Conference</u>:

1. S. Basak, **A. Chattopadhyay** and B. Dey, **"**Design and Implementation of a 8-bit Processor Using FSM Modeling in VHDL,**"** *in Proc. of the First Indian Conference on Trends in Modern Engineering Systems* **(*IConTiMES-2008*)**, Kalyani, West Bengal, *Feb. 23-24, 2008*, pp. 74-82.

2. **A. Chattopadhyay** and A. Mallik, "Dual-Material Gate Insulator for Tunnel Field-Effect Transistor," *in Proc. of the International Conference on Communication, Computers and Devices* ***(ICCCD)****, Dec. 10-12, 2010, Kharagpur, India.*

3. **A. Chattopadhyay** and A. Mallik, "The Impact of a High-κ Gate Dielectric on a p-Channel Tunnel Field-Effect Transistor," *in Proc. of the 16th International Workshop on Physics of Semiconductor Devices* ***(IWPSD)***, *Dec. 19-22, 2011, Kanpur, India.*

4. S. Guin, **A. Chattopadhyay,** A. Karmakar, and A. Mallik, "Effects of a Pocket Doping in a Schottky-Barrier MOSFETs," *in Proc. of the 1st Winter Workshop on Engineering at Nanoscale: From Materials to Bio-sensors, Dec. 10-12, 2012, Indore, India.*

5. A. Mallik and **A. Chattopadhyay,** "Spacer-Drain Overlap Dependence of Subthreshold Characteristics for Tunnel Field-Effect Transistors Based on Vertical Tunneling," *in Proc. of the 1st International Conference on Emerging Electronics* ***(IEEE-ICEE)****, Dec. 15-17, 2012, Bombay, India.*

6. S. Guin, **A. Chattopadhyay,** A. Karmakar, and A. Mallik, "Influence of a Pocket Doping in a Schottky Tunneling FET," *in Proc. of the 11th International Meeting for Future of Electron Devices, Kansai* ***(IEEE-IMFEDK),*** *Jun. 5-6, 2013,Osaka, Japan.*

7. A. Basu, S. Sinha Roy, and **A. Chattopadhyay**, "Implementation of a spatial domain salient region based digital image watermarking scheme," *in Proc. of the 2nd International Conference on Research*

in Computational Intelligence and Communication Networks ***(ICRCICN)****, Sept. 23-25, 2016, Kolkata, India.*

8. E. Datta, **A. Chattopadhyay**, and A. Mallik, "Effect of Gate Dielectric Material on the Analog Performance of a Ge-Source Tunnel FET," *in Proc. of 19th International Workshop on the Physics of Semiconductor and Devices* ***(IWPSD),*** *Dec.12-15, 2017, Delhi, India.*

9. S. Sinha Roy, A. Basu, M. Das, and **A. Chattopadhyay**, "FPGA Implementation of an Adaptive LSB Replacement Based Digital Watermarking Scheme," *in Proc. of the International Symposium on Devices, Circuits and Systems* ***(ISDCS)***, *Mar. 29-31, 2018, Howrah, India* [ISBN: 978-1-5386-5122-3].

10. A. Bhattacharyya, P. S. Gupta, and **A. Chattopadhyay**, "Comparative Performance Analysis between Junctionless and Conventional FET Based Biosensor," *in Proc. of the 5th International Conference on Microelectronics, Circuits and Systems* ***(Micro-2018)****, May 19-20, 2018, Bhubaneswar, India* [ISBN: 81-85824-46-1].

11. Z. Haque, A. Saha, T. S. Das, A. Basu, and **A. Chattopadhyay**, "Performance Evaluation of Audio Watermarking in EMD Framework," *in Proc. of 4th International Conference on Research in Computational Intelligence and Communication Networks* ***(ICRCICN)***, *Nov. 22–23, 2018, Kolkata, India* [ISBN: 978-1-5386-7638-7].

(iii) Book Chapter:

1. S. Sinha Roy, A. Basu, and **A. Chattopadhyay**, "Hardware Implementation of a Visual Image Watermarking Scheme using Qubit/Quantum Computation through Reversible Methodology", *Quantum-Inspired Intelligent Systems for Multimedia Data Analysis,* ***IGI Global***, ch.4, pp. 95-140, Apr. 2018 [DOI: 10.4018/978-1-5225-5219-2.ch004].

2. E. Datta, **A. Chattopadhyay**, and A. Mallik, "Effect of Gate Dielectric Material on the Analog Performance of a Ge-Source Tunnel FET", *The Physics of Semiconductor Devices*, ***Springer,*** ch. 104, pp. 675-680, Feb. 2019 [DOI: https://doi.org/10.1007/978-3-319-97604-4_104].

(iv) Book:

1. S. Sinha Roy, A. Basu, and **A. Chattopadhyay**, "Intelligent Copyright Protection for Images," ***CRC Press*** *(Taylor & Francis Group),* Apr. 2019 [ISBN: 978-0-367-19817-6].

Language Known :

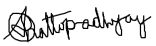
Name of the Language	Speak	Read	Write
Bengali	Yes	Yes	Yes
English	Yes	Yes	Yes
Hindi	Yes	No	No

Interests & Activities :

Hobbies : Watching & Playing Cricket
Extra Activities : Practicing Yoga
Skills : Eager, hard-working, responsible and possessing excellent personal skills to motivate and boost confidence amongst others

Declaration :

I do hereby solemnly declare that the statements made above are true and correct to the best of my knowledge and belief.



Date : 22/09/2019 **Signature**

Place: Shyamnagar, West Bengal