Dr. Soumya Pandit

Assistant Professor, Stage-III,
Institute of Radio Physics and Electronics,
University of Calcutta,
and
Chartered Engineer [India],
Electronics and Telecommunication Engineering,
Office Address: 92, Acharya Prafulla Chandra Road,
Kolkata 700 009, India
Residential Address: 168, Rajdanga School Road,
P.O. East Kolkata Township,
Kolkata 700107, India

Email: sprpe@caluniv.ac.in
soumya.pandit.rpe@gmail.com

Mobile: +91 9874852007
Website: https://drsoumyapandit.in

Vision and Objectives

Vision: To serve society and humanity through delivering education.

Objectives:

- To contribute to the Indian Semiconductor Mission of the Govt. of India in building a vibrant semiconductor design and innovation ecosystem to enable India's emergence as a global hub for electronics manufacturing and design in a more structured, focused, and comprehensive manner.
- To contribute to Indian Higher Education in developing 85,000 skilled manpower in VLSI Chip design over next 5 years.
- To contribute to indigenous Intellectual Property (IP) generation and encourage, enable and incentivize Transfer of Technologies (ToT).
- To develop collaborations programs with national and international agencies, industries and institutions for catalysing collaborative research and skill development.

- To refurbish the M.Tech. program in VLSI Design at the University of Calcutta to[2] cater to the needs of students in terms of employability.

Professional Summary

- Acquired the Ph.D. degree in the domain of VLSI Design from the Indian Institute of Technology, Kharagpur in the year 2009.
- Joined the Institute of Radio Physics and Electronics in the capacity of Assistant Professor in 2008.
- Developed the ASIC Design Laboratory at the University of Calcutta.
- Chief Investigator of the Special Manpower Development Program, Chips to System Design, funded by Ministry of Electronics and Information Technology, Govt. of India at the University of Calcutta since 2015.
- Established the 180nm CMOS Technology Flow and taped out VLSI chips at 180nm CMOS Technology, first time in the University of Calcutta.
- Successfully completed 5 sponsored research projects, funded by MeitY, Govt. of India, DST-SERB, TEQIP etc as principal investigator.
- Collaboration with IIT Kharagpur, IIEST Shibpur, NIT Silchar, NIT Durgapur and Jadavpur University.
- Supervised 1 Ph.D. student, 1 student submitted Ph.D. thesis and 2 others are working.
- Supervised 26 nos of M.Tech. project works in the various areas of VLSI Design.
- Authored 1 book, 12 nos of book chapters, 20 nos of journal papers and 36 nos conference proceedings.
- Delivered more than 30 numbers of invited talks at various international conferences, seminars and workshops.
- Conducted 3 summer schools, funded by UGC Networking Resource Centre in Physical Sciences as course director or course joint director and 1 Mini Colloquium and several numbers of seminars and technical lectures funded by IEEE.
- Member of technical committee of various international conferences like International Conference on VLSI Design, VLSI Design and Test Symposium, Indicon, COMSYS to name a few.
- Co-ordinator of 2-Year M.Tech. (FT) in VLSI Design and 3-Year M.Tech (PT) in VLSI Design.
- Teach post-graduate level courses like Algorithms for VLSI Design, Testing and Verification of VLSI Circuits, CAD Techniques Laboratory (IC Design), Advanced Engineering Mathematics
- Teach undergraduate courses like Linear Integrated Circuits, Statistics and Probability Theory, Circuit Theory Lab
- Founded the IEEE Electron Devices Society University of Calcutta Student Branch Chapter as chapter advisor.
- Chartered Engineer (India) in Electronics and Telecommunication Engineering Division of the Institution of Engineers (India)
- Fellow of IETE (India)
- Regional Editor, R-10 of IEEE Electron Devices Society Newsletter.

Skills

- Analog IC Design and Simulation using SPICE
- EDA Tools like Cadence, Mentor Graphics, Synopsys Custom IC Design for installation of the tool, establishing client-server license architecture in RHEL 6/ Cent OS 7.
- Managing 180nm CMOS Process Development Kit of various fabrication industries like SCL, National Semiconductor (now Texas Instruments)
- Management of LAN
- Project Finance Accounting using EXCEL and other packages.
- Documentation of reports.
- Editorial Management in conferences using tools like EasyChair and Microsoft CMT.

Education

- 2009 Ph.D. in Engineering, Indian Institute of Technology, Kharagpur,
  Ph.D. Thesis Title: An Optimization-based Methodology for High-Level Design of Analog Systems
- 2002 M.Tech in Radio Physics and Electronics, University of Calcutta, Obtained 1st Class
- 2000 M.Sc in Electronic Science, University of Calcutta, Obtained 1st Class
- 1998 B.Sc with Honours in Physics, University of Calcutta, Obtained 1st Class

Employment Details

- 2017 (Feb)-onwards
  Assistant Professor, Stage-III
  Institute of Radio Physics and Electronics
  University of Calcutta
- 2012 (Feb)-2017 (Feb)
  Assistant Professor, Stage-II
  Institute of Radio Physics and Electronics
  University of Calcutta
- 2008 (Nov)- 2012 (Feb)
  Assistant Professor, Stage-I
  Institute of Radio Physics and Electronics
  University of Calcutta
- 2008 (Feb)-2008 (Oct)
  Assistant Professor
  Electronics and Communication Engineering Department
  Meghnad Saha Institute of Technology
- 2003 (Aug)-2008 (April) Research Consultant

- 2002 (Jan)-2003 (July) Lecturer
  Electronics and Communication Engineering Department
  Meghnad Saha Institute of Technology

Current Academic Responsibilities:

- Co-ordinator 2 years Full time M.Tech VLSI Design and 3 years Part time M.Tech VLSI Design program of the University of Calcutta.
- Teacher –In Charge of IC Design Laboratory, a research and post-graduate level teaching laboratory.
- Teacher-In Charge (jointly) of Electronic Circuits Laboratory and Analog Circuits Simulation, undergraduate level teaching laboratory.
- Joint teacher-incharge, VLSI Design Laboratory, Dept. of Radio Physics and Electronics
- Member of the Syllabus sub-committee responsible for up gradation of B.Tech syllabus in Electronics and Communication Engineering at the Institute of Radio Physics and Electronics
- Member of the Syllabus sub-committee responsible for upgradation of M.Tech VLSI Design syllabus.
- Member of the Board of Studies in Electronics and Communication Engineering and Board of Post Graduate Studies in VLSI Design
- Member of Admission and Selection Committee for M.Tech students admission.
- Member of the Departmental Committee.

Research Interest

- Intelligent Analog Circuit Design.
- Ultra - Low Power Design of Analog ICs
- Compact Modeling of Advanced Semiconductor Devices for VLSI Applications
- Data Analytics and Machine Learning for VLSI Applications

Professional Memberships

- Senior Member, IEEE, Membership No: 80057634
- Chartered Engineer, Electronics and Telecommunication Engineering India, M-165437-8
- FOSET, Life Member, Membership No: LM/2011-2104
- Fellow IETE, F-502172

Involvements in IEEE

- Founded the IEEE Electron Devices Society Student Branch Chapter, University of Calcutta[5] (SBC28561A) in the capacity of chapter advisor
- Treasurer, IEEE EDS Calcutta Chapter 2012-2013
- Chair, IEEE EDS Calcutta Chapter, 2014-2015
- Members of the Regions and Chapter Committee, IEEE Electron Devices Society, USA, 2016-2017, 2020 onwards.
- Vice Chair, SRC, Region-10, IEEE Electron Devices Society, USA, 2018- 2020
- Regional Editor, R-10 IEEE EDS Newsletter

Few Other Professional Achievements

- Member of the Board of Studies in Electronics and Communication Engineering, National Institute of Science and Technology, Berhampur, Autonomous College under Biju Pattanaik University of Technology, Odhisa.
- Session Chair, 5th International Conference on Opto-Electronics and Applied Optics (OPTRONIX-2019)
- Session Chair, Modeling and Simulation Track, 4th IEEE International Conference on Emerging Electronics (ICEE), 16-19 Dec, 2018
- Member of the Technical Program Committee, 31st International Conference on VLSI Design, 2018
- Member of the Technical Program Committee, 21st International Symposium on VLSI Design and Test, 2017, IIT Roorkee
- Member of the Technical Program Committee, 7th International Symposium on Embedded Computing and System Design, 2017, NIT Durgapur
- Ph.D. Forum Chair, 29th International Conference on VLSI Design, 2016
- Session Chair, International Conference, Microelectronics, Circuits and Systems (Micro-2014), International Conference, Microelectronics, Circuits and Systems (Micro-2014)6

Research Publications

Book

1. S.Pandit, C.Mandal and A.Patra, Nano-Scale CMOS Analog Circuits: Models and CAD Techniques for High-Level Design, CRC Press, USA, Taylor & Francis, UK and others, 2014, Print ISBN: 978-1-4665-6426, eBook ISBN: 978-1-4665-6428-2

Journals

1. S.K.Maity, P.Dutta and S.Pandit, 'Compact drain current modeling of planar InGaAs quantum well MOSFET', Micro and Nano Structures, Elsevier, Volume 169, September 2022, Date: 13.08.2022 Pages: 207361, 1-14, **IF = 3.22**, https://doi.org/10.1016/j.micrna.2022.207361
2. S.K.Maity and S.Pandit, 'Device-circuit analysis of ultra-thin body In1−xGaxAs on insulator MOS transistor with varying indium mole fraction and channel thickness', Engineering Research

Express, IoP Science 4 (2022) 025024, Date: 20.05.2022, https://doi.org/10.1088/2631-6 8695/ac6ecc, Online ISSN: 2631-8695 Scopus and WoS indexed, Science Citation Index Expanded journal, UGC Care-List Group **II IF = 1.205**

3. K.Mukherjee, T.Sau, S.Upadhyay, S.Mitra, A.Bhowmik, S.Sarkhel, S.Pandit, R.K.Pal, 'A 588 nW, 1 nA current reference circuit with extremely low (0.002%/V) line sensitivity over a wide supply voltage range and low temperature coefficient' International Journal of Numerical Modeling: Electronic Networks, Devices and Field, John Willey and Sons, Date: 18.03.2022, https://doi.org/10.1002/jnm.2999, Scopus and WoS indexed, Science Citation Index Expanded journal, UGC Care-List Group II, **IF=1.054**
4. S.K.Maity and S.Pandit, 'A SPICE compatible physics-based intrinsic charge and capacitance model of InAs-OI-Si MOS transistor'. Superlattices and Microstructures Page No: 106975: 1-13 Date: August 2021, Superlattices and Microstructures, Volume 156, August 2021, 106975, https://doi.org/10.1016/j.spmi.2021.106975 , ISSN: 0749-6036, Scopus and WoS indexed, Science Citation Index Expanded journal, UGC Care-List Group II **IF = 2.658**
5. S.Sengupta and S.Pandit, 'A Unified Model of Drain Current Local Variability due to Channel Length Fluctuation for an n-channel Eδ DC MOS Transistor', Silicon, Springer Vol 14, https://doi.org/10.1007/s12633-021-01218-w, Page No: 4979-4989, Date: 31.07.2021, Electronic ISSN 1876-9918, Print ISSN 1876-990X, Scopus and WoS indexed, Science Citation Index Expanded journal, UGC Care-List Group II, **IF = 2.941**
6. S.K.Maity and S.Pandit, 'Performance Assessment of CMOS circuits using III ‑ V on Insulator MOS Transistors', Silicon, Springer, Vol. 13, . https://doi.org/10.1007/s12633-020-00582- , Page No: 1939–1949, Date: 13.09.2020, Electronic ISSN 1876-9918, Print ISSN 1876-990X, Scopus and WoS indexed, Science Citation Index Expanded journal, UGC Care-List Group II, **IF = 2.941**
7. S.K.Das, D.Das and S.Pandit, 'A Global Routing Method for Graphene Nanoribbons Based Circuits and Interconnects', ACM Journal on Emerging Technologies in Computing Systems Vol. 16 Issue 3 July 2020 https://doi.org/10.1145/3384214, Page No: 31:1-31:28 Date: 22.05.2020, ISSN:1550-4832, EISSN:1550-4840, Scopus and WoS indexed, Science Citation Index Expanded journal, UGC Care-List Group II, **IF = 1.420**
8. S. K. Maity, A. Haque and S. Pandit, "Charge-Based Compact Drain Current Modeling of InAs-OI-Si MOSFET Including Subband Energies and Band Nonparabolicity," in IEEE Transactions on Electron Devices, vol. 67, no. 6, pp. 2282-2289, June 2020, doi: https://10.1109/TED.2020.2984578 Scopus and WoS indexed, Science Citation Index Expanded journal, UGC Care-List Group II, **IF = 3.222**
9. S.K.Maity and S.Pandit, 'Analysis of scaling of thickness of the buffer layer on analog/RF and circuit performance of InAs ‑ OI ‑ Si MOSFET using NQS model', International Journal of Numerical Modeling: Electronic Networks, Devices and Field, John Willey and Sons, Page no 1-16, Date: 31.07.2019, Scopus and WoS indexed, Science Citation Index Expanded journal, UGC Care-List Group II, **IF:1.054**, https://doi.org/10.1002/jnm.2664
10. S. Sengupta and S. Pandit, "Analysis of Drain Current Local Variability of an n-Channel E δ DC MOSFET Due to RDD Considering Inversion Charge and Correlated Mobility Fluctuations," in IEEE Transactions on Electron Devices, vol. 65, no. 4, pp. 1267-1275, April 2018, doi: https://10.1109/TED.2018.2808299 Scopus and WoS indexed, Science Citation Index Expanded journal, UGC Care-List Group II, **IF = 3.222**
11. S.K.Maity and S.Pandit, 'Effects of BOX Engineering on Analog/RF and circuit performance of InGaAs-OI-Si MOSFET', Page no 777-1794, Date: 13th July 2017, International Journal of

Electronics, Taylor and Francis, UK, ISSN 0020-7217 (Print); ISSN 1362-3060 (Online),7 Scopus and WoS indexed, Science Citation Index Expanded journal, UGC Care-List Group II, **IF=1.227**

12. S.K.Maity and S.Pandit, Study of G-S/D underlap for enhanced analog performance and RF/circuit analysis of UTB InAs-OI-Si MOSFET using NQS small signal model, Superlattice and Microstructure, Elsevier, 2016. http://dx.doi.org/10.1016/j.spmi.2016.11.053 Page No: 362-372, Date: 01.02.2017, ISSN: 0749-6036, Scopus and WoS indexed, Science Citation Index Expanded journal, UGC Care-List Group II, **IF = 2.658**
13. R.Das, A.K.Gond, S.Sengupta and S.Pandit, Study of temperature variation on threshold voltage and sub-threshold slope of EδDC MOS transistor including quantum corrections and reduction Techniques, Microsystem Technologies, Springer, Vol. 23, No 9, 2017, DOI https://10.1007/s00542-016-2995-z , Page No: 4221–4229, Scopus and WoS indexed, Science Citation Index Expanded journal, UGC Care-List Group II, **IF = 2.658**
14. S.Sengupta and S.Pandit, Substrate Bias Effect of Epitaxial Delta Doped Channel MOS Transistor for Low Power Applications, International Journal of Electronics, Taylor and Francis, UK, Vol. 104, No 1, ISSN 0020-7217 (Print); ISSN 1362-3060 (Online), Scopus and WoS indexed, Science Citation Index Expanded journal, UGC Care-List Group II, IF = 1.457, https://doi.org/10.1080/00207217.2016.1180546
15. S. Sengupta and S. Pandit, "Channel Profile Design of Eδ DC MOSFET for High Intrinsic Gain and Low VT Mismatch," in IEEE Transactions on Electron Devices, vol. 63, no. 2, pp. 551-557, Feb. 2016, doi: https://10.1109/TED.2015.2507065, ISSSN No: 0018-9383, Scopus and WoS indexed, Science Citation Index Expanded journal, UGC Care-List Group II, **IF = 3.222**
16. S.Sengupta and S.Pandit, Study of performance scaling of 22nm epitaxial delta-doped channel MOS transistor', International Journal of Electronics, Taylor and Francis, UK, 0020-7217 (Print), 1362-3060 (Online) , Page No: 967-981 Date: 12.08.2014, Scopus and WoS indexed, Science Citation Index Expanded journal, UGC Care-List Group II , **IF = 1.457**
17. J.Mukhopadhyay and S.Pandit, Modeling and Design of a Nano Scale CMOS Inverter for Symmetric Switching Characteristics, Volume 2012 | Article ID 505983 | https://doi.org/10.1155/2012/505983 Hindwai, Pages: 1-13 Date: 22.04.2012
18. S.Pandit, C. Mandal and A.Patra, A Methodology for Generation of Performance Models for the Sizing of Analog High-Level Topologies, VLSI Design, vol. 2012, Article ID 505983, Hidwai. ISSN: 1065-514X (Print), ISSN: 1563-5171 (Online) doi: https://10.1155/VLSI Pages: 1-1 Date: 15.09.2011,
19. S.Pandit, C.Mandal and A.Patra, An Automated High-Level Topology Generation Procedure for Continuous-Time ΣΔ Modulator', Integration, the VLSI journal, 2010, Vol. 43 Pages: 289-304, Date: 04.03.2010
20. S. Pandit, S. K. Bhattacharya, C. Mandal and A. Patra, "A Fast Exploration Procedure for Analog High-Level Specification Translation," in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 27, no. 8, pp. 1493-1497, Aug. 2008, doi: https://10.1109/TCAD.2008.925785. Scopus and WoS indexed, Science Citation Index Expanded journal, UGC Care-List Group II **IF: 2.565**

Book Chapters

S. No	Chapter Title with Page No	Details Publication (Text/Reference/Subject Books/Chapter in Books)	ISSN/ISBN No
1.	Characterization of Stochastic Process Variability Effects on Nano-Scale Analog Circuits	**Chapter in Book, Book Title** Nanoelectronics for Next-Generation Integrated Circuits Edited By Rohit Dhiman, Taylor and Francis/CRC Press	9781003155751
2.	Design Methodology for Ultra-Low-Power CMOS Analog Circuits for ELF-SLF Applications **Page No: 23–43**	**Chapter in Book, Book Title** Dhiman, R., Chandel, R. (eds) Nanoscale VLSI. Energy Systems in Electrical Engineering. Springer, Singapore. https://doi.org/10.1007/978-981-15-7937-0_2	Print ISBN 978-981-15-7936-3 Online ISBN 978-981-15-7937-0
3.	CMOS Design and Analysis of Four Quadrant Analog Multiplier Circuit for LF Applications **Page No: 279–289** **Date: 17.12.2019**	**Chapter in Book, Book Title:** Lecture Notes in Electrical Engineering, vol 602, Springer, Singapore, Kundu, S., Acharya, U., De C., Mukherjee S. (eds) https;//doi.org/10/1007/978-981-15-0829-5_28. Date: 17.12.2019	Print ISBN 978-981-15-0828-8 Online ISBN 978-981-15-0829-5
4.	UTB III-V-OI-Si MOS Transistor: the future transistor for VLSI Design **Date:** September 2019 **Pages: 27-46**	**Chapter in Book, Book Title:** VLSI and Post-CMOS Electronics, Edited by Rohit Dhiman, Rajeevan Chandel, IET, UK	ISBN-13: 978-1-83953-053-1
5.	Design of a Health Monitoring System for Heart Rate and Body Temperature Sensing Including Embedded Processing using ARM	**Chapter in Book, Book Title:** Advances in Intelligent Systems and Computing, vol 999. Springer, Singapore, Das A., Nayak J., Naik B.,	Print ISBN 978-981-13-9041-8, Online ISBN

	Cortex M3 **Page No: 93-103**	Pati S., Pelusi D. (eds)	978-981-13-9042-5
6.	Smart Health Monitoring System for Temperature, Blood Oxygen Saturation, and Heart Rate Sensing with Embedded Processing and Transmission Using IoT Platform, **Page no: 81-92**	**Chapter in Book, Book Title:** Advances in Intelligent Systems and Computing, vol 999. Springer, Singapore, Das A., Nayak J., Naik B., Pati S., Pelusi D. (eds)	Print ISBN 978-981-13-9041-8, Online ISBN 978-981-13-9042-5
7.	Variability in Nano-scale MOS Transistor and EδDC MOS Transistor **Page no 25-48**	**Chapter in Book, Book Title**: Nanoscale Devices: Physics, Modeling and their Application, Editor: B.K.Kaushik, Chapter 2, Publisher: CRC Press, USA, 16 November 2018	ISBN: 9781138060340 eBook ISBN 9781315163116
8.	Behavioral Modeling of Differential Inductive Seismic Sensor and Implementation of its Read Out Circuit, Pages **253-262**	**Chapter in Book, Book Title**: Communication, Devices, and Computing, Editor: Jaydeb Bhaumik Indrajit Chakrabarti Bishnu Prasad De Banibrata Bag Surajit Mukherjee, Springer Lecture Notes in Electrical Engineering, Vol. 470, April 2018. Publisher: Springer	ISBN 978-981-10-8585-7
9.	Nanoscale MOSFET: MOS Transistor as Basic Building Block **Page: 145–172** **Date: 02.09.2015**	**Chapter in Book, Book Title**: Introduction to Nano: Basics to Nanoscience and Nanotechnology, 2015 Publisher: Springer, Editor A.Sengupta and C.K.Sarkar.	ISBN 978-3-662-47314-6
10.	An Improved gm/ID Methodology for Ultra-Low-Power Nano-Scale CMOS OTA Design **Pages: 128–137** **Date: 2013**	**Chapter in Book, Book Title**: Manoj Singh Gaur Mark Zwolinski Vijay Laxmi Dharmendra Boolchandani Virendra Singh Adit D. Singh (Eds.), CCIS 382, pp. 128–137, 2013. Publisher: Springer-Verlag Berlin Heidelberg 2013	ISSN 1865-0929 e-ISSN 1865-0937 ISBN 978-3-642-42023-8 e-ISBN 978-3-642-42024-5 DOI 10.1007/978-3-642-42024-5
11.	Statistical Characterization of Flicker Noise Fluctuation of a Nano-Scale	Advanced Nanomaterials and Nanotechnology Editor: P.K.Giri et al	ISBN No: 978-3-642-34215-8

	NMOS Transistor **Page no 203-214** https://doi.org/10.1007/978-3-642-34216-5_21	Publisher: Springer-Verlag Berlin Heidelberg 2013	
12.	MOSFET Characterization for VLSI Circuit Simulation **Page no: 267-362**	Technology Computer Aided Design: Simulation for VLSI MOSFET Editor: Chandan Kumar Sarkar Publisher: CRC Press, USA, May 2013	ISBN No: 978-1-4665-1265-8

Conference Proceedings

S. No	Paper Title.	Proceedings Details	ISSN/ISBN No
1.	Reduction of Interconnect Delay and Resistance While Minimizing Grid Area in GNR Based VLSI Routing Problem	Proceedings of 5th International Symposium on Devices, Circuits and Systems, Publisher: IEEE	
2.	Reliability Aware Global Routing of Graphene Nanoribbon Based Interconnect	Proceedings of 26th International Symposium on VLSI Design and Test	
3.	Statistical Analysis of a Low Power Analog Current Source **Pages:** 160-164, doi: 10.1109/VLSIDCS53788.2022.9811473. **Date:** 04.07.2022	Proceedings of 2022 IEEE VLSI Device Circuit and System (VLSI DCS), 2022 Publisher: IEEE	Electronic ISBN:978-1-6654-3801-8 Print on Demand(PoD) ISBN:978-1-6654-3802-5
4.	A 0.6 V 1.6 nA Constant Current Reference Circuit with Improved Power Supply Sensitivity **Date: 21.06.2021** **Pages:** 498-503, doi: 10.1109/DevIC50843.2021.9455885.	Proceedings of 2021 Devices for Integrated Circuit (DevIC), Publisher: IEEE, Editor:	Electronic ISBN:978-1-7281-9955-9 Print on Demand(PoD) ISBN:978-1-7281-9956-6
5.	Minimization of Switching Activity of Graphene Based Circuits **Pages**: **139-144, doi:**	Proceedings of 2021 34th International Conference on VLSI Design and 2021 20th	Electronic ISBN:978-1-6654-4087-5

	10.1109/VLSID51830.2021.00029. **Date: 26.04.2021**	International Conference on Embedded Systems (VLSID), 2021, Publisher: IEEE	Print on Demand(PoD) ISBN:978-1-6654-3127-9
6.	Comparative Study of Doublet OTA Circuit Topologies Operating in Weak Inversion Mode for Low Power Analog IC Applications **Date: 28.08.2020** **Pages:** 74-78, doi: 10.1109/VLSIDCS47293.2020.9179858.	Proceedings of 2020 IEEE VLSI DEVICE CIRCUIT AND SYSTEM (VLSI DCS), 2020, Publisher: IEEE	Electronic ISBN:978-1-7281-1933-5 Print on Demand(PoD) ISBN:978-1-7281-1934-2
7.	Crosstalk Aware Global Routing of Graphene Nanoribbon Based Circuits **Pages**: **243-248,** doi: 10.1109/NANO46743.2019.8993935 **Date: 13.02.2020**	Proceedings in 2019 IEEE 19th International Conference on Nanotechnology (IEEE-NANO) Publisher: IEEE	Electronic ISBN:978-1-7281-2892-4 USB ISBN:978-1-7281-2891-7 Print on Demand(PoD) ISBN:978-1-7281-2893-1
8.	Compact drain current modeling of InAs-OI-Si MOS transistor including quantum confinement, **Page no. 1-5, doi: 10.1109/ISDCS.2018.8379654**.	Proceedings of ISDCS-2018, Editor, H. Rahaman, Publisher: IEEE Publishers, USA	Electronic ISBN: 978-1-5386-5122-3 USB ISBN: 978-1-5386-5121-6 Print on Demand(PoD) ISBN: 978-1-5386-5123-0
9.	Design and Analysis of a CMOS Analog Multiplier as part of Read Out Circuit for a differential Inductive Seismic Sensor, **Pages 1-6**	Proceedings of CCSN-2017, Issue of publication – Vol-1, Editor: D.Acharya, Publisher: IASTM	ISBN-81-85824-46-0,
10.	Study of LER/LWR Induced VT	Proceedings of Dev IC 2017,	Electronic

	Variability of an EδDC n-channel MOS Transistor **Date: 19.10.2017** **Pages: 685-689**	Publisher: IEEE, Editor: Dr. Angsuman Sarkar Sandip Nandi	ISBN:978-1-5090-4724-6 Print on Demand(PoD) ISBN:978-1-5090-4725-3
11.	Study of Short Channel Characteristics of Gate Underlapped InGaAs-OI-Si MOS Transistor **Date: February 2016** **Pages:**	Proceedings of NCDC 2016, Editor: A.K.Panda, Publisher: IPM Pvt. Ltd, Odhisha	ISBN: 978-93-82208-78-5
12.	Effect of Buried Oxide (BOX) Thickness Scaling on Analog/RF Performance of InGaAs-on-Insulator MOS Transistor	Proceedings of 2nd Int. Conf. Microelectronics, Circuits and Systems, organized by IASTM, Editor: D.Acharya, Publisher: Arisha Creation, Kolkata	ISBN: 81-85824-46-0
13.	Temperature Analysis of Threshold Voltage and Sub-threshold slope of Epitaxial Delta Doped Channel MOS Transistor for SoC Applications, **Pages: 105-109**, Date: 2015	Proceedings of 2nd Int. Conf. Microelectronics, Circuits and Systems, organized by IASTM, Editor: D.AcharyaPublisher: Arisha Creation, Kolkata	ISBN: 81-85824-46-0
14.	Amino acid classification based on Electrical response of its Codon composition **Pages: 279-284** **Date: 17.03.2016**	Proceedings of IEEE Int. Conference on Research in Computational Intelligence and Communication Networks, Pp279-284, 2015, Editor Siddhartha Bhattacharyya, Nibaran Das, Ujjwal Maulik, Debotosh Bhattacharjee, Indrajit Pan, Hrishikesh Bhaumik, Anirban Mukherjee and Kazumi Nakamatsu,	Electronic ISBN:978-1-4673-6735-6 CD:978-1-4673-6734-9
15.	Study of Wide Temperature Variation (100-500 K) on Drain Current Characteristics of a 22nm n-channel EδDC MOS Transistor	Proceedings of 4th International. Conference on Computing, Communication and Sensor Network, 2015, organized by IASTM, Editor: D.Acharya, Publisher: IASTM	ISBN: 81-85824-46-0
16.	Impact of Gate Underlap on Analog/RF Performance of InGaAs-OI-Si Substrate MOS Transistor for SoC Computing Applications	Proceedings of 4th International. Conference on Computing, Communication and Sensor Network 2015, organized by IASTM, Publisher: IASTM	ISBN: 81-85824-46-0

17.	Study of Analog and RF Performance of UTB-OI-Si Substrate MOS Transistor using Buffered InGaAs and Silicon Channel **Pages. 1-4** **Date: 06.04.2017**	Proceedings of 6th International Conference on Computers and Devices for Communication (CODEC) 2015, Publisher: IEEE	Electronic ISBN: 978-1-4673-9513-7 CD-ROM ISBN: 978-1-4673-9511-3 Print on Demand(PoD) ISBN: 978-1-4673-9514-4
18.	Power Aware Clustering and Placement for FPGAs	1st International Science and Technology Congress, IEMCON 2014, Publisher: Elsevier	ISBN: 9789351072485
19.	Study of Reverse Substrate Bias Effect of 22nm node Epitaxial Delta Doped Channel MOS Transistor **Pages: 1-6** **Date: 21.08.2014**	VLSI Design and Test, 18th International Symposium on, Publisher: IEEE	Electronic ISBN: 978-1-4799-4006-6 Print ISBN: 978-1-4799-5088-1 CD-ROM ISBN: 978-1-4799-4007-3
20.	Threshold Voltage Modeling of Deeply Depleted Channel MOSFET and Simulation Study of its Analog Performances **Pages. 1-4** **Date: 17.03.2014**	Electronics, Communication and Instrumentation (ICECI), 2014 International Conference, Publisher: IEEE	Electronic ISBN: 978-1-4799-3983-1 CD-ROM ISBN: 978-1-4799-3982-4
21.	Statistical Characterization of Flicker Noise Fluctuation of a Nano-Scale NMOS Transistor **Page no 203-214** https://doi.org/10.1007/978-3-642-34216-5_21	Advanced Nanomaterials and Nanotechnology Editor: P.K.Giri et al Publisher: Springer-Verlag Berlin Heidelberg 2013	ISBN No: 978-3-642-34215-8
22.	Semi-Analytical Estimation of Intra-Die Variations of Analog Performances of Nano-scale NMOS Transistor **Page No 854904-1-5.**	16th IWPSD, Proceedings SPIE edited by Y N. Mohapatra, B. Mazhari, M. Katiyar, Vol. 8549 (SPIE, Bellingham, WA, 2012)	ISSN: 0277-786X ISBN: 9780819493002
23.	Performance Modeling of Nano-scale CMOS Inverter Circuit using Least Square Support Vector Machine **Page 61-64**	Proceedings of Int. Conf. ICNB 2011	

24.	'Effects of Intra-Die Process Variations on Nano-scale CMOS Analog Circuit Performances' **Page No: 165-168**	Proceedings of Int. Conf. ICNB 2011	
25.	'An Analytical Approach for Statistical Modeling of the Effect of Process Parameter Variation on the Performance of Nano-scale CMOS VCO' **Page No: 18-27**	Proceedings of International Conference, ICFANT 2010 Jadavpur University, Kolkata December 2010	
26.	'Statistical Study of the Effect of Process Variations on Nano-scale CMOS Circuits with Scaling' **Pages**. 1-4, doi: 10.1109/INDCON.2010.5712724. **Date: 14.02.211**	Proceedings of IEEE Indicon 2010 Kolkata, December 2010 Publisher:IEEE	Electronic ISBN: 978-1-4244-9074-5 Print ISBN: 978-1-4244-9072-1 CD-ROM ISBN: 978-1-4244-9073-8
27.	An Artificial Neural Network-based Approach for Performance Modeling of Nano-scale CMOS Inverter **Page No: 165-170**	Proceedings of Int. Conf. IEMCON 2011 January 2011 Publisher: IEEE	ISSN: 2296-6611
28.	Design of a Nano-scale CMOS Inverter with Symmetric Switching Characteristics using Particle Swarm Optimization Algorithm' **Pages: 536-540**	Proceedings of Int. Conf. IEMCON 2011 January 2011 Publisher: IEEE	ISSN: 2296-6611
29.	A Methodology for Sizing of Analog High-Level Topologies using Computational Intelligence Techniques', ICETES 2010 (*awarded best paper),* **Pages: 520-523**	Proceedings of International Conf. in Emerging Trends in Engineering Technologies 2010 Noorul Islam University, Kumaracoil, Tamilnadu March 2010, Publisher: Noorul Islam University.	Print ISSN: 9443217158
30.	Statistical Simulation and Modeling of Nano-scale CMOS VCO using Artificial Neural Network **Date: 22.02.2011**	**Chapter in Book, Book Title**: Proceedings of IEEE VLSI Design Conference, New Delhi January 2010, Publisher: IEEE	ISSN: 1063-9667

	Pages: 94-99 **doi: 10.1109/VLSID.2011.28.**		
31.	Systematic Methodology for High-Level Performance Modeling of Analog Systems **Pages 361 - 366**	Proceedings of IEEE International Conference on VLSI Design January 2009, Publisher: IEEE	ISSN: 1063-9667 Print ISBN: 978-0-7695-3506-7
32.	'A Hybrid Search procedure for System Level Analog Design Space Exploration Used in High Level Synthesis of Analog Systems' , **Pages: 114-117**	Proceedings of Int. Conf. CODEC 2006 Publisher: IEEE	ISSN: 978-81-8465-152-2
33.	A Formal Approach for High Level Synthesis of Linear Analog Systems, **Pages:345-348**	Proceedings of ACM Int. Conf. GLSVLSI 2006, Publisher: IEEE	ISSN: 1-59593-347-6
34.	'High Level Synthesis of Higher Order Continuous Time State Variable Filters with Minimum Sensitivity and Hardware Count', pp 1203 - 1204	**Chapter in Book, Book Title**: Proceedings of IEEE/ACM Int. Conf. DATE 2006, Publisher: IEEE	Print ISBN: 3-9810801-1-4 ISSN: 1530-1591
35.	'High Level Synthesis of Linear Analog Systems', , **Pages 389-392**	Int. Conf. EAIT 2005 Elsevier Pub	
36.	'Porous Silicon device Modeling and Linearization Technique', **Pages: 145-148**	IEEE Int. Conf. EDSSC 2003, Publisher: IEEE	ISSN: 0-8803-7749-4/03

Ongoing and Completed Research Projects and Consultancies

S.No	**Title**	**Agency**	**Period**	**Grant/Amount Mobilized (Rs. Lakh)**	
1.	Special Manpower Development Programme-Chip to Systems Design in VLSI Design	MeitY, Govt. of India	2015-2021	2015-2016	16.95
				2016-2017	0
				2017-2018	17.25
				2018-2019	15.35

				2019-2020	25.06478
				2020-2021	14.36449
2.	Modern Biology and Signal Processing Group,	University with Potential for Excellence, Calcutta University	2017-2019	2017	4.5
				2019	1.5
3.	Development of a design automation tool for nano CMOS analog circuits	DST, Govt. of India	2010-2013	Rs. 12,12,000/-	
4.	Device-Circuit Co-design and Integration of Device CAD and Circuit CAD for the study of Nano-scale MOS Transistors for Low Power SoC Applications	TEQIP, Phase-II, University of Calcutta	November 2013-November 2015	Rs. 1 Lakh	
5.	Statistical Modeling, Design and Optimization of Nano-CMOS Analog/RF Circuits	CRNN, University of Calcutta	2009-2011	Rs. 2 Lakh + Salary of 1 SRF	

Research Guidance

Ph.D Supervision

Sr. No	Name of the Ph.D. Student	Degree Awarded	Thesis Submitted (Yes/No), Thesis Title
1.	Mrs. Sarmista Sengupta	Yes	Yes. Thesis Title: Study of Process Variability Effects on EδDC MOS Transistor for Low Power VLSI Applications
2.	Mr. Subir Maity	No	Yes. Thesis Title: Studies on Device and Circuit Performance of III-V-OI-Si MOS Transistors
3.	Mr. Subrata Das	No	Studies on Physical Design of VLSI Circuits based on Graphene Nanoribbon.

4.	Mrs. Koyel Mukherjee	No	Ultra-Low Power Analog IC Design	17

M.Phill/M.Tech.

Sr. No	Name of the Student	Dissertation Title	Degree Awarded
1.	Saroj Mondal	E123_Core Micro-Architecture	YES 2009
2.	Sipra Mandal	Modeling, Simulation and Design of a Nano-scale CMOS Circuits using Soft Computing Techniques	YES 2010
3.	Chandan Mukherjee	Statistical Study of the Variation of Process Parameters on the Performance of CMOS VCO and OPAMP Circuits	YES 2010
4.	Kaustav Dasgupta	Design and Study of Digital Phase Locked Loop using nanoscale CMOS Technology	YES 2010
5.	Krishnendu Dey	Design of a Wide-band, Low-Power Digital Phase Locked Loop using 32-nm CMOS Technology	YES 2010
6.	Dipankar Dhabak	Performance Modeling of Nano-scale CMOS Logic Circuits using Soft Computing Techniques	YES 2011
7.	Joyjit Mukherjee	Design of a Nano-scale CMOS Inverter Circuits using Soft Computing Techniques	YES 2011
8.	Debabrata Bose	Design of a nano-scale CMOS Inverter using Generic Algorithm.	YES 2011
9.	Somnath Paul	Design of Amplifier for Ultra-Low Power Analog Application using nano-scale MOS Transistors	YES 2012
10.	Abhijit Dana	SPICE Modeling and Parameter Extraction of Nano-scale MOS Transistors for Low Power Analog Circuit Applications	YES 2012
11.	Pranjal Barman	Statistical Study of Random Discrete Dopant Effect in Scaled MOS Transistor and Its Reduction by Channel Engineering Approach.	YES
12.	Kritanjali	Study of Analog Performances of Nano-scale MOS Transistors	YES

	Das		
13.	DebayanBairagi	Study of Substrate Bias Effect for Epitaxial Delta Doped Channel MOS Transistor	YES 2014
14.	Aparna Das	Study of Power Aware Clustering for FPGA	YES 2014
15.	Mousumi Ghosh	Study of Power Aware Placement for FPGA	YES 2014
16.	Rahul Kumar Shaw	Design of a Low Power Front End OTA and PSO Application for the Optimization of Threshold Voltage Parameter of EδDC Transistor	Yes 2016
17.	Rinkee Das	Temperature Characterization over Wide Range (100-500K) of an n-channel EδDC MOS Transistor	Yes 2016
18.	Saswata Chatterjee	Design of a Low Frequency, Low Power, Fast Locking Digital Phase Locked Loop using SCL 180 nm technology	Yes 2017
19.	Suman Goswami	Adaptive Noise Cancellation of Seismic Signal using Least Mean Square Algorithm and Implementation using FPGA	Yes 2017
20.	Kaushik Sen	Modeling of a Differential Inductive Seismic Sensor and its Simulation using COMSOL Multiphysics	Yes 2017
21.	Monalisa Dutta	Design and Implementation of FPGA Based Earthquake Early Warning System	YES 2017
22.	Sirsha Guha	Temperature Analysis of Device Performance of a sub-50nm p-channel FinFET	YES 2019
23.	Srabanti Saha	Implementation of Multi-Phase DC-DC Bulk Converter	YES 2020
24.	Sayantan Chanda	Evaluation of On-Chip Solution for Scan Bus Width Reduction on Large SoC	YES 2021
25.	Anindita Das	Electromigration-aware Physical Design Automation of Multi-million Gate Chip	YES 2021
26.	Raya Adhikary	Design of a Low Noise Instrumentation Amplifier for Sensor Applications	YES 2022

Fellowships and Awards

Sr. No	Award Name	Academic Body
1.	Best Paper Award for the Paper A Methodology for Sizing of Analog High-Level Topologies using Computational Intelligence Technique	Noorul Islam University
2.	Visiting Scientist at Nanoscale Device Modeling and Characterization Laboratory, 21st-30th June 2018	IIT Kanpur
3.	Chartered Engineer (India), Electronics and Telecom Engineering Div. M-165437-8, Dated: 11.07.2019	The Institution of Engineers, India
4.	Fellow of the The Institution of Electronics and Telecommunication Engineers, F-502172, dated13th February 2021	IETE, India

Invited Lectures/Papers presented

S. No	Title of Lecture/Academic Session	Title of Conference/Seminar etc	Organized by	Whether international/ national
1.	Process Variability in Nano-scale CMOS Analog Circuits	Keynote Talk, IEEE VLSI DCS 2022, 26th-27th February 2022.	IEEE EDS Student Branch Chapter Meghnad Saha Institute of Technology	International
2.	Unified Model for Drain Current Local Variability in MOS Transistors	4th IEEE International Conference on Emerging Electronics, 16-19th December 2018, Bangalore, India	IEEE Electron Devices Society	International
3.	Variability in MOS Transistors	3rd International Conference on Devices and Circuits, March 2019	Kalyani Govt. Engineering College	International
4.	Process Variability Modeling and Low Leakage Device Design in IoT Design Space"	IEEE EDS Technical Talk, Monday, 25th June 2018	Electrical Engineering Department, IIT Kanpur	National
5.	Design and Implementation of an FPGA	Paper presented at 31st International Conference on VLSI Design and 17th	VLSI Society of India	International

	based Hardware for Seismic Event Detection in an EEW System	Int. conf on Embedded Systems **held from 6th to 10th Jan 2018** in Pune, India		
6.	VLSI Circuit Testing and Testability	Invited Talk at 4th National Conference on Devices and Circuits, **24th February 2018**	NIST Berhampur	National
7.	Overview of Nano-scale MOSFETs	One Day Seminar on Electron Devices and Applications 2018, **20th March, 2018**	Dept. of ECE, IEEE EDS Students Branch Chapter, Netaji Subhas Engineering College	National
8.	Tutorial on CMOS Analog IC Design	2 day Workshop on Emerging VLSI Techologies	Assam University, Silchar	National
9.	Invited Talk:Epitaxial Delta Doped Channel MOS Transistor: A Candidate for Smart Mobile SoC Applications	2nd International Conference on Microelectronics, Circuit and Systems, July 11, 2015	International Association of Science, Technology and Management,	International
10.	Invited Talk: Advanced MOS Transistor for Mobile SoC Design,	International Workshop on Advanced Electron Devices and Circuits,	IEEE EDS Calcutta Chapter and School of Electronics Engineering, KIIT University, 3rd-4th December 2014.	Internatioal
11.	Invited Talk: Short Channel Effects in MOS Transistors	1day Workshop on Advanced Semiconductor Device Modeling and Fabrication	Abacus Institute of Engineering and Management, 15th November 2014.	National
12.	Keynote Talk: Nano-scale CMOS Analog Circuits: Essential Challenges and Design Methodologies,	International Conference, Microelectronics, Circuits and Systems (Micro-2014)	International Association of Science, Technology and Management, Puroshottam Institute of Engineering and Technology, Rourkela, Odisha and IETE, Kolkata. 11th July 2014.	International
13.	Session Chair	International Conference,	International Association of	International

		Microelectronics, Circuits and Systems (Micro-2014)	Science, Technology and Management, Puroshottam Institute of Engineering and Technology, Rourkela, Odisha and IETE, Kolkata. 11th July 2014.	
14.	Invited Talk: *Electron System Design and Manufacturing*	Seminar on Embedded System and VLSI	Elitte Institute of Engineering and Management, 29th March 2014	National
15.	Joint Course Director, Winter School	UGC-NRCPS Sponsored Winter School Physics and Technology of Sensors (PHYTSENS-12)	University of Calcutta 26th November 2012	National
16.	*MEMS Capacitive Sensors*	UGC-NRCPS Sponsored Winter School Physics and Technology of Sensors (PHYTSENS-12)	University of Calcutta 26th November 2012	National
17.	*Interface Electronics for Smart Sensors*	UGC-NRCPS Sponsored Winter School Physics and Technology of Sensors (PHYTSENS-12)	University of Calcutta 22nd November 2012	National
18.	*MOSFET Characterization for VLSI Circuit Simulation*	Faculty Development Program on Recent Trends on VLSI Design and Embedded Systems	C.V.Raman College of University, BPUT, Orissa 27th July 2012	National
19.	Device Characterization for VLSI Circuit Simulation	UGC-NRCPS Sponsored summer school Nano Mastd 2012,	University of Calcutta 1st June 2012	National
20.	CMOS Analog Circuits	UGC-NRCPS Sponsored summer school Techniques for Design, Fabrication and Computation of Integrated Circuits (TECHNOMICS-12)	University of Calcutta 29th May 2012	National
21.	Low Power CMOS Circuits	----------do----------	-----do---------	National
22.	Performance Modeling, Parameter Extraction Technique and Statistical	International Workshop on Device Modeling of Microsystems	MOS-AK/GSA and INAE during March 16-18, 2012 at JIIT, Noida	International

	Modeling of Nano-scale CMOS Transistors for VLSI Circuit Simulation			
23.	Low Power CMOS Circuits	'Advances in Photonic, Electronic and Communication Systems (APECS-2012)'	Tezpur University, Date: January 24th 2012	National
24.	Parameter Extraction Technique for MOS Modeling	Advances in Electronics, Communication and Information Technology	Mizoram University Date: March 25th 2011	National
25.	Low power CMOS Design: Sources and Minimization Techniques	Advances in Electronics, Communication and Information Technology	Mizoram University, Date: March 24th 2011	National
26.	Performance Modeling of Nano Scale CMOS Inverter Circuit using Least Squares Support Vector Machine	International Conference on Nanotechnology and Biosensor (ICNB2-2011)	Raghu Engineering College, Visakhapatnam (A.P), India	International
27.	Effects of Intra-Die Process Variations on Nano-Scale CMOS Analog Circuit Performance	International Conference on Nanotechnology and Biosensor (ICNB2-2011)	Raghu Engineering College, Visakhapatnam (A.P), India	International
28.	Statistical Modeling of Process Variability Effects on Nano-scale CMOS Analog and RF Circuits	IEEE Technical Talk	IEEE Calcutta Section, EDS Chapter, 22nd June 2010	National
29.	CAD for Nano CMOS Analog Design	Frontiers of Electronics and Communication	North Eastern Regional Institute of Science and Technology (NERIST),	National

			Nirjuli, Arunachal Pradesh, 8th September 2009	
30.	CMOS Device Modeling for Analog and Digital Circuits	Summer School NanoDev 3rd June 2009	UGC-NRCPS, IRPE	National
31.	UML based Object Oriented Methodology for Analog Test Structure Design Automation	9th IEEE VLSI Design and Test	VLSI Society of India	National

I declare that the information provided are true to the best of my knowledge and documentary evidence for each information will be produced as and when required.

(Soumya Pandit)