Curriculam Vitae

Name of the Faculty : **Dr.SuchismitaTewari**
Designation : **Assistant Professor**
e-mail : **suchi_tewari@yahoo.co.in**

1. Academic record:

Degree	Board/University/subject	Comment
B. SC (Physics Hons.)	University of Calcutta	1st class
B.Tech (Radio Physics and electronics)	University of Calcutta	1st class
M. Tech (VLSI design)	University of Calcutta	Gold medallist
Ph.D	University of Calcutta	

2. Research and other Experiences:

a) **Service experience**: in Tech Mahindra Limited as Technical Associate
(From October 17, 2008 to May 22, 2009)
b) **Research experience:** CSIR- SRF (June 1, 2012- February 17, 2016)
c) **Teaching experience:** Assistant Professor (Institute of Radio Physics & Electronics, University of Calcutta) (February 18, 2016 - till date)

3. Journal papers`

i. **S. Tewari,** A. Biswas, and A. Mallik, "Study of InGaAs-channel MOSFETs for analog/mixed-signal system-on-chip applications,"***IEEE Electron Device Lett*.,** vol. 33, no.3, pp. 372-374, March 2012. (**Impact factor = 3.03**).
ii. **S. Tewari,** A. Biswas, and A. Mallik, "Impact of different barrier layers and Indium content of the channel on the analog performance of InGaAsMOSFETs,"***IEEE Trans. Electron Devices*,**vol. 60, no.5, pp.1584-1589, May 2013 (**Impact factor = 2.358).**
iii. **S. Tewari,** A. Biswas, and A. Mallik, "Investigation on High Performance CMOS With p-Geand n-InGaAs MOSFETs for Logic Applications, "***IEEE Trans. NanoTechnology,***vol. 14, no.2, pp.275-281, March 2015 (**Impact factor = 1.619**).
iv. **S. Tewari,** A. Biswas, and A. Mallik, "Performance of CMOS With Si p-MOS and Asymmetric InP/InGaAs n-MOS for Analog Circuit Applications**,"** ***IEEE Trans. Electron Devices***vol. 62, no.5, pp.1655-1658, May 2015 (**Impact factor = 2.358**).
v. **S. Tewari,** A. Biswas, and A. Mallik, "Performance of CMOS With Si p-MOS and Asymmetric InP/InGaAs n-MOS for Analog Circuit Applications**,"** ***IEEE Trans. Electron Devices***vol. 63, no.6, pp.2313-20320, June 2016 (**Impact factor = 2.358**).

vi. S. De, **S. Tewari,** A. Biswas, and A. Mallik"Impact of channel thickness and spacer length on logic performance of p-Ge/n-Si hybrid CMOSFETs for ULSI applications" Superlattices and microstructures, vol. 109, pp.316-323, 2017 **(Impact factor = 2.145**).

vii. K. Banerjee, **S. Tewari**, and A. Biswas, "Impact of aspect ratio of nanoscale hybrid p-Ge/n-Si complementary FinFETs on the logic performance," Microsystem Technologies, 2017. (Impact factor =1.195)

viii. **S. Tewari**, S. De, A. Biswas, and A. Mallik, "Impact of sidewall spacer on n-InGaAs devices and hybrid InGaAs/Si CMOS amplifiers in deca-nanometer regime," Microsystem Technologies, 2017. (Impact factor =1.195)

ix. N. Mandal, S. Tewari, A. Biswas, "Enhancement of pH-sensitivity using $In_{0.53}Ga_{0.47}As$ channel ion-sensitive-field-effect-transistors," Microsystem Technologies, 2018 (Impact factor = 1.195)

x. S. De, S. Tewari, A. Biswas, A. Mallik, "Improved digital performance of hybrid CMOS inverter with Si p-MOSFETand InGaAs n-MOSFET in the nanometer regime," Microelectronics Engineering, vol. 211, pp. 18-25, 2019 (Impact factor = 2.02)

4. Conference proceedings/presentation:

i. **S. Tewari,** A. Biswas, and A. Mallik, "Analog Performance Analysis of Inversion Type Enhancement Mode n-MOSFETs Using InGaAs Channel," 2nd International Conference on Nanotechnology and Biosensors (ICNB-2) 2011, pp. 180-184, December 28-29, 2011, Visakhapatnam.

ii. **S. Tewari,** A. Biswas, and A. Mallik, "Influence of a Barrier layer in Enhancement Mode n-MOSFETs Using InGaAs Channel For Analog/Mixed-Signal System-on-Chip Applications," International Conference on Electrical and Electronics Engineering(ICEEE-2012), pp. 74-76, August 12, 2012, Hyderabad ***(This paper received "Young Investigator Award Certificate").***

iii. **S. Tewari,** A. Biswas, and A. Mallik, "Analog Performance of Dual-Material Gate InGaAs MOSFETs International Conference on Emerging Electronics (ICEE-2012), pp. 1-4, December 15-17, 2012 (IIT Bombay).

iv. **S. Tewari,** A. Biswas, and A. Mallik, "Impact of Indium Contents on the Analog Circuit Performance of InGaAs channel MOSFETs," International Conference on Electrical, Electronics and Computer Science (ICEECS-2013), March 24, 2013 Chandigarh.

v. **S. Tewari**, A. Biswas, and A. Mallik, "Studies on Digital Performance of CMOS Comprising Ge p-MOSFET and InGaAs n-MOSFET with Different In Contents," 2nd International Conference on Innovations in Electronics and Communication Engineering (ICIECE -2013), pp.667-671, August 9-10, 2013, Guru Nanak Institutions, Hyderabad ***(This paper received "Best Paper Award Certificate").***

vi. S. De**, S. Tewari,** A. Biswas, and A. Mallik, "Studies on the Analog Performance of InGaAsChannelJunctionless Transistors," 2nd International Conference on Innovations in Electronics and communication Engineering(ICIECE-2013), pp. 676-680, August 9-10, 2013, Hyderabad ***(This paper received "Best Paper Award Certificate").***

vii. **S. Tewari**, A. Biswas, and A. Mallik,"Effects of Channel Barrier Layer On the Analog Performance of p-Ge/n-InGaAs CMOS Devices,"2nd International conference on Emerging Technology, Trends in Electronics, Communication & Networking, 26-27 December, 2014, Surat.

viii. **S. Tewari,** P. K. Saha,A. Biswas, and A. Mallik, "Investigations on the Logic Performance of Hybrid CMOSFETs Comprising p-Ge/ n-InGaAs MOSFETs with Barrier Layers," on International conference on microelectronics computing and communication systems (MCCS-2015), November 14-15, 2015, Advanced Regional Telecom Training Center BSNL, Near Jumar River Bridge, Hazaribag Road, Ranchi-835217, Jharkhand, India

ix. S. De, **S. Tewari**, A. Biswas, and A. Mallik, "Improved logic circuit performance of hybrid CMOS inverter with Si p-MOSFET and InGaAs n-MOSFET. "International conference on

recent trends in engineering and material sciences (ICEMS-2016), 17-19 March, 2016**,** Jaipur National University, Jaipur, India.

x. **S. Tewari**, A. Biswas, and A. Mallik, "Investigations on Logic Performance of p-Ge/n-Si Hybrid CMOSFETs for Digital Applications." 2nd International conference on Nano-electronics, Circuits & Communication Systems (NCSS),December 25-26, 2016, Advanced Regional Telecom Training Center BSNL, Near Jumar River Bridge, Hazaribag Road, Ranchi-835217, Jharkhand, India.

xi. **S. Tewari**, S. De, A. Biswas, and A. Mallik, "Effect of sidewall spacers on the analog performance of InGaAsnMOSFETs in deca-nanometer regime, " 4th International Conference on 'Microelectronics, Circuits and Systems', (MICRO) June 3-4, 2017.

xii. K. Banerjee, **S. Tewari,** A. Biswas, and A. Mallik, "Analysis of logic performance of nanoscale hybrid p-Ge/n-Si complementary FinFETs," 4th International Conference on 'Microelectronics, Circuits and Systems', (MICRO) June 3-4, 2017.

xiii. N. Mondal, S. Munshi, **S. Tewari,** and A. Biswas, "Analysis of high pH-sensor using $In_{0.53}Ga_{0.47}As$ channel ion-sensitive-field-effect-transistors," 5th International Conference on 'Microelectronics, Circuits and Systems', (MICRO) May 19-20, 2018.

xiv. S. De, **S. Tewari,** A. Biswas, "Negative bias temperature instability (NBTI) effects on p-Si/n-InGaAs hybrid CMOSFETs for digital applications**"** International Conference on Recent Trends on Electronics & Computer Science (ICRTECS-2019) March 18-1, 2019 .

5. Awards:

i. Young Investigator Award Certificate (ICEEE-2012).
ii. Best paper Award certificate (ICIECE-2013).
iii. Co-author of a Best Paper Award certificate winning paper (ICIECE-2013).
iv. Best paper Award certificate 1st prize (MICRO-2017).
v. Best paper Award certificate 1st prize (MICRO-2018).

5. Professional activities:

i.Life member of Indian Physical Society (Membership no: LM/1053)

ii. Ex Vice-chairperson of IEEE, University of Calcutta, student branch