DEBASRI SAHA

Assistant Professor

A. K. Choudhury School of Information Technology
Technology Campus, University of Calcutta
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Specialization: Hardware Security, VLSI Design and Optimization, FPGA

Academic qualification:

University/ Institute from which degree is awarded	Degree	Year
Indian Statistical Institute	PhD in CS	2012
University of Calcutta	MTech in CSE	2006
University of Calcutta	BTech in CSE	2004
University of Calcutta	BSc in Physics Honours	2001

Professional Details:

- Assistant Professor, Stage II (May, 2017 – till date), Stage I (May, 2013 –May, 2017), A. K. Choudhury School of Information Technology, University of Calcutta

- Assistant Professor, Department of Computer Science and Engineering, IIT Patna (July, 2012-April, 2013)

- Senior Research Fellow (July, 2008 – June, 2012), Junior Research Fellow (July, 2006 – June, 2008), Advanced Computing and Microelectronics Unit, Indian Statistical Institute, Kolkata

Research Interests: Hardware IP security in VLSI and embedded systems, VLSI design optimization, meta-heuristic techniques, FPGA, power distribution network, speech enhancement techniques.

Title of my PhD Thesis: On Trusted Sharing of Intellectual Property of VLSI Design.

PhD Advisor: Prof. Susmita Sur-Kolay, Indian Statistical Institute, Kolkata

Research Projects:

- Co- Principle Investigator for the following Project brought in collaboration with Indian Statistical Institute (ISI), Kolkata, India.
  Project title: An efficient framework for ensuring security of FPGA-based application cores in Cloud and IoT environment
  Granting Authority: DST, GoI Amount: About Rs. 25 lacs Duration: 2019-2022
- Steering Committee member for the project, where parent institute is IIT Kharagpur.

Project title: Special Manpower Development Programme for Chips to System Design (SMDP III-C2SD), Granting Authority: MeitY

Research Guidance:

Principal advisor of the following PhD Students, jointly advised by Prof. Amlan Chakrabarti

- Moumita Chakraborty, was in DST INSPIRE fellowship, PhD awarded by CU in Dec, 2020
- Tanmay Biswas, in DST Rajiv Gandhi Fellowship, thesis submitted to CU in 2019
- Krishnendu Guha, in DST INSPIRE fellowship, thesis to be submitted to CU
- Amit Saha, DST fellowship, PhD registered under CU in 2017

Visit Abroad:

- Visited School of Computing, National University of Singapore, Singapore for research discussions and exploration of collaboration during February 21-28, 2019.
- Visited Nanyang Technological University, Singapore within the above mentioned period for the same purpose.

Tutorial Talk:

- Half-day tutorial talk at International Conference on VLSI Design and Embedded Systems (VLSID), co-presented with Prof. Susmita Sur-Kolay, Indian Statistical Institute on January 6, 2019
  Title: Hardware Security of Embedded Systems and IoT Environment
- Half-day tutorial talk at International Symposium on VLSI Design and Test Symposium (VDAT) co-presented with Prof. Susmita Sur-Kolay, Indian Statistical Institute on July 1, 2012
  Title: Intellectual Property Protection and Security of ICs

Publications:

Book Chapter:

1. *Debasri Saha* and Susmita Sur-Kolay, FPGA-based IP and SoC Security, in the book `Fundamentals in IP and SoC Security' edited by Swarup Bhunia, Sandip Ray and Susmita Sur-Kolay, Springer, Feb. 2017.

Journal:

1. Krishnendu Guha, Atanu Majumder, Debasri Saha, Amlan Chakrabarti:
Dynamic power-aware scheduling of real-time tasks for FPGA-based cyber physical systems against power draining hardware trojan attacks. J. Supercomput. 76(11): 8972-9009 (2020)

2. Krishnendu Guha, Debasri Saha, Amlan Chakrabarti, Stigmergy-Based Security for SoC Operations From Runtime Performance Degradation of SoC Components, *ACM Transactions on Embedded Computing Systems (TECS)*, Vol. 18, No. 2, pp. 14:1-14:26, 2019.

3. Debasri Saha, Susmita Sur-Kolay, Guided GA-based Multiobjective optimization of placement and assignment of TSVs in 3D ICs, *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, (Early Access), 2019.

4. Tanmay Biswas, Sudhindu Bikash Mandal, *Debasri Saha*, Amlan Chakrabarti, FPGA based dual Microphone speech enhancement, Microsystem technologies, Vol 25, no. 3, Springer Berlin-Heidelberg, pp. 765-775, 2019.

5. Moumita Chakraborty, Debasri Saha, Amlan Chakrabarti, Sayani Bindai, A CAD approach for pre-layout optimal PDN design and its post-layout verification, *Microprocessors and Microsystems - Embedded Hardware Design*, Elsevier, Vol. 65, pp. 158-168, 2019

6. Krishnendu Guha, *Debasri Saha*, Amlan Chakrabarti, Real-Time SoC Security against Passive Threats Using Crypsis Behavior of Geckos, *ACM Journal on Emerging Technologies in Computing Systems (JETC)*, Vol 13, no. 3, pp. 41:1-41:26, 2017

7. Tanmay Biswas, Sudhindu Bikash Mandal, *Debasri Saha*, Amlan Chakrabarti, Coherence based dual microphone speech enhancement technique using FPGA, *Microprocessors and Microsystems - Embedded Hardware Design*, Vol. 55, pp. 111-118, 2017

8. *Debasri Saha*, Susmita Sur-Kolay, Embedding signatures in Reconfigurable scan architecture of SoC Design, *Journal of IET Computers and Digital techniques (IET CDT)*, Vol 10, No. 3, pp. 110-118, 2016 (available in IEEE Xplore).

9. *Debasri Saha*, Susmita Sur-Kolay, Watermarking in Hard Intellectual Property for Pre-Fab and Post-Fab Verification, *IEEE Transactions on VLSI (TVLSI) Systems*, Vol 23, No. 5, pp. 801-809, 2015.

10. Moumita Chakraborty, Amlan Chakrabarti, Partha Mitra, *Debasri Saha*, Pre-layout decoupling capacitance estimation and allocation for noise-aware crypto-system on-chip applications, *Journal of Low Power Electronics (JOLPE)*, Vol 11, No, 3, pp. 333-339, 2015.

11. *Debasri Saha*, Susmita Sur-Kolay, Secure Public Verification of IP Marks in FPGA Design through a Zero-Knowledge Protocol, *IEEE Transactions on VLSI (TVLSI) Systems*, Vol. 20, No. 10, pp. 1749-1758, 2012.

12. Pritha Banerjee, *Debasri Saha*, Susmita Sur-Kolay, Cone based Placement for FPGAs, *Journal of IET Computers and Digital techniques (IET CDT)*, vol 5, no. 1, pp. 49-62, 2011 (available in IEEE Xplore).

13. *Debasri Saha*, Susmita Sur-Kolay, Robust Intellectual Property Protection of VLSI Physical Design, *Journal of IET Computers and Digital techniques (IET CDT), Vol 4, No. 5*, pp. 388-399, 2010 (available in IEEE Xplore).

14. *Debasri Saha*, Susmita Sur-Kolay, SoC: A Real Platform for IP Reuse, IP Infringement and IP Protection, *Journal of VLSI Design*, special issue '*CAD for Gigascale SoC Design and Verification Solutions'*, Hindawi Publishing Corporation, USA, vol 2011, article id 73195, 2011, (available in ACM portal).

15. Rajat K. Pal, *Debasri Saha*, Samar Sen Sarma, A Memetic Algorithm for Computing a Nontrivial Lower Bound on Number of Tracks in Two-Layer Channel Routing, *Journal of Physical Sciences* (ISSN: 0972-8791), vol. 11, pp. 199-210, 2007.

Conference:

1. Krishnendu Guha, Debasri Saha, Amlan Chakrabarti: Blockchain Technology Enabled Pay Per Use Licensing Approach for Hardware IPs. DATE 2020: 1618-1621

2. Krishnendu Guha, Debasri Saha, Amlan Chakrabarti: A Multi-Agent Co-operative Model to Facilitate Criticality based Reliability for Mixed Critical Task Execution on FPGA based Cloud Environment. VLSI Design 2020: 143-148

3. Krishnendu Guha, Debasri Saha, Amlan Chakrabarti: Zero Knowledge Authentication for Reuse of IPs in Reconfigurable Platforms. TENCON 2019: 2040-2045

4. Krishnendu Guha, Atanu Majumder, *Debasri Saha*, Amlan Chakrabarti, Reliability Driven Mixed Critical Tasks Processing on FPGAs Against Hardware Trojan Attacks, 21st Euromicro. Conf of Digital System Design (DSD), Czech Republic, 2018, pp. 537-544

5. Krishnendu Guha, *Debasri Saha*, Amlan Chakrabarti, SARP: Self Aware Runtime Protection Against Integrity Attacks of Hardware Trojans, VLSI Design and Test (VDAT), 2018, pp. 198-209

6. Tanmay Biswas, Subhadeep Bhattacharjee, Sudhindu Bikash Mandal, *Debasri Saha*, Amlan Chakrabarti, FPGA-based novel speech enhancement system using microphone activity detector, Advanced Computing and Systems for Security (ACSS), 2018, pp. 117-127.

7. *Debasri Saha*, Susmita Sur-Kolay, Multi-objective optimization of placement and assignment of TSVs in 3D ICs, Intl. Conf. on VLSI design and Embedded Systems (VLSID), 2017, pp. 373-377.

8. Krishnendu Guha, *Debasri Saha*, Amlan Chakrabarti, Self aware SoC security to counteract delay inducing hardware Trojans at runtime, Intl. Conf. on VLSI design and Embedded Systems (VLSID), 2017, pp. 417-422

9. Moumita Chakraborty, Debasri Saha, Amlan Chakrabarti, A CAD approach for on-chip PDN with power and supply noise reduction for multi-voltage SOCS in pre-layout stage, Intl. Symposium on Embedded Computing and System Design (ISED), 2017, pp. 1-4

10. Moumita Chakraborty, Amlan Chakrabarti, Partha Mitra, Debasri Saha, Krishnendu Guha, Pre-layout module wise decap allocation for noise suppression and accurate delay estimation of SoC, VLSI Design and Test (VDAT), 2016, pp. 1-6

11. Krishnendu Guha, *Debasri Saha*, Amlan Chakrabarti, RTNA: Securing SOC architectures from confidentiality attacks at runtime using ART1 neural networks, VLSI Design and Test (VDAT), 2015, pp. 1-6.

12. Debasri Saha, Adaptive Multi-layer Routing for Incremental Design of an SoC, Frontiers in Intelligent Computing, Theory and Application, (FICTA), 2015, pp. 657-665.

13. *Debasri Saha*, Susmita Sur-Kolay, Trusted Sharing of Intellectual Property in Electronic Hardware Design, Workshop on Embedded System Security (WESS), A workshop of Embedded System Week (ESWEEK), 2014, pp. 9:1-9:3.

14. Moumita Chakraborty, Krishnendu Guha, Amlan Chakrabarti and *Debasri Saha,*Analysis of Secret Key Revealing Trojan Using Path Delay Analysis for some Cryptocores, Frontiers in Intelligent Computing, Theory and Application, (FICTA), 2014, pp. 13-20.

15. Moumita Chakraborty, Krishnendu Guha, Amlan Chakrabarti and *Debasri Saha*, Analysis of Power Distribution Network for some Cryptocores, 3rd Intl. Conf. on Advances in Computing, Communication and Informatics (ICACCI), 2014, pp. 2618-2622.

16. *Debasri Saha* and Susmita Sur-Kolay, Updation of Activation Sequence of a Chip after its Deployment for Access Control, Intl Conf on Computational Intelligence: Modeling, Techniques and Applications (CIMTA) 2013, pp. 373-380.

14. *Debasri. Saha*, Susmita Sur-Kolay, Planarization of Metal Layers in a Chip based on Voronoi Diagram, in Prof. Int'l Conference on Computers and Devices for Communications (CODEC), IEEE CS press, 2012.

15. *Debasri. Saha*, A Resilient Authentication and Trojan Detection Technique for Hard IP, Int'l Conference on Communication Computers and Security (ICCCS), 2012, pp. 24-30, Procedia technology (available in ScienceDirect)

16. *Debasri. Saha*, Susmita Sur-Kolay, Pre and Post Fabrication Protection for DFM Enhanced Layout, accepted in *IEEE Latin American Symposium on Circuits and Systems* (LASCAS), 2011.

17. *Debasri. Saha*, Susmita Sur-Kolay, A Unified Approach for IP Protection across Design Phases in a Packaged Chip, In *Proc. IEEE International. Conference. on VLSI Design*, 2010 (VLSID), pp. 105-110.

18. *Debasri Saha*, Susmita Sur-Kolay, Secure Leakage-Proof Public Verification of IP Marks in VLSI Physical Design, In *Proc. IEEE Computer Society Annual Symposium on VLSI* (ISVLSI), Tampa, Florida, 2009, pp 169-174.

19. *Debasri Saha*, Susmita Sur-Kolay, Encoding of Floorplans through Deterministic Perturbation, In *Proc. IEEE International Conference on VLSI Design* (VLSID), 2009, pp 315-320.

20. *Debasri Saha*, Susmita Sur-Kolay, An Analytical Approach to Direct IP Protection of VLSI Floorplans, In *Proc. IEEE Intl. Conference on Industrial and Information System* (ICIIS), 2008.

21. *Debasri Saha*, Susmita Sur-Kolay, Fast Robust Intellectual Property Protection for VLSI Physical Design, In *Proc IEEE International Conference on Information Technology* (ICIT), 2007, pp 1-6. (**Best paper award**).

22. *Debasri Saha*, Pritha Banerjee, Susmita Sur-Kolay, Fast I/O Pad Placement in FPGAs, In *Proc. of IEEE VLSI Design and Test Symphosium* (VDAT), 2007, pp. 152-161.

23. *Debasri Saha*, Parthasarathi Dasgupta, Susmita Sur-Kolay, Samar Sen Sarma, A novel scheme for encoding and watermark embedding in VLSI Physical Design for Intellectual Property Protection, In *Proc. International Conference on Computing: Theory and Application* (ICCTA'07), 2007, pp 111-116

24. *Debasri Saha*, Watermarking Graph Coloring Problem, In Proc. *IEEE WIE National Symposium on Emerging Technologies* (WieNSET), 2007.

25. *Debasri Saha*, Rajat K. Pal, Samar Sen Sarma, A Memetic Algorithm for Refinement of Lower Bound of Number of Tracks in Channel Routing Problem, *IFIP International Federation for Information Processing, Vol. 228, Intelligent Information Processing III*, 2006, pp. 307-316.

Membership in Profession Bodies:

- Senior Member, IEEE
- Member, International Association of Engineers (IAENG)
- Member, The Association of Computer Electronics and Electrical Engineers (ACEEE)
- Working as Program or organizing Committee Member for IEEE conferences and others:
    - PC member for Intl. Conference on VLSI Design and Embedded Systems (VLSID) in consecutive five years 2014, 2015, 2016, 2017 and 2018.
    - PC member for Intl. Symposium on VLSI Design and Test Symposium (VDAT) in 2017 and 2019.
    - OC member for VLSID in 2016.
    - PC member for ACSS in 2015

Awards:

- Best Paper Award in International Conference on Information Technology (ICIT), 2007.
- National Scholarship in 2001 for the results in Physics Honours.
- GATE Scholarship in 2004.

Other notable activities:

- Working as reviewer for many IEEE Transactions, conferences and others as follows:

IEEE Transactions on VLSI Systems (TVLSI), IEEE Transactions on Information and Forensic Security (IFS), IEEE Transactions on Multi-scale Computing (TMSCS), IET Computers & Digital Techniques (IET CDT), Springer journal Hardware and System Security (HASS), Integration the VLSI Journal, Microelectronics Journal, ACM Journal of Emerging Technologies (JETC);
Several IEEE conferences VDAT'19, VLSID'18, VLSID'17, VDAT'17, VLSID'16, VLSID'15, VLSID'14, IHCI'12, ITC'12, VLSID'09, VDAT'09, VDAT'07, ICCTA'07, ICIT'07 etc

- Imparted training twice to Interra Engineers:

Schedules: 25-29 Oct, 2010 and 18-22 July, 2011. Tools: ICstation from Mentor Graphics, Talus from Magma and open source FEL (fedora electronic laboratory).

Conducted laboratory sessions on Physical Design in Summer School on Fundamentals of Digital Design Automation, held at ISI on 22-26 July 2014, organized by ACMU, ISI and IEEE WIE Kolkata Section. Tools: ICstation from Mentor Graphics, Talus.